FUNCTION

Resolver sensor

VHDL File

resolver.vhd

Applicable Devices

Spartan3ADSP, Spartan6, 7-family, UltraScale+

Xilinx primitive used

-

Sub modules used

atan2.vhd
dsp48a4m.vhd

Execution time

1,36 cycles

Introduction

The Resolver sensor IP core provides elaboration for the analog data acquired from resolver sensor. The output is the electric angle. It is provided of a linear interpolation unit to generate intermediate values between consecutive hall commutation events.

Detailed Description

The sensor itself and required electronic interface is expensive compared with hall sensors or incremental encoder, so the choice to use resolver is usually limited to robust application. The sensor works with analog sine wave signals so the positioning (distance from sensor to electronic), cabling quality and electronic interface shall be accurate to avoid noise injection on analog signals that can disturb the acquisition and influence the motor control software.

The resolver IP described in this document is developed to interface the common three signals sensor:

1) Exciter winding: a fixed frequency sine wave signal is generate by interface to resolver IP,
2) Cosine winding: direct output,
3) Sine winding: quadrature output.

The resolver characteristics: exciter frequency/amplitude, transfer ratio, pair poles, impedances of windings, maximum mechanical speed are defined in resolver documentation.

The resolver IP support the single pair poles resolver class in which a complete 360 degrees sine/cosine output wave for each mechanical revolution. This class is specific designed for high speed application.

The multi pair poles resolver class is not supported.

The choice of resolver type is strictly application depend. The supplied IP can operate at very high speed and the output angle precision is about 20 bits.

Resolver angle evaluation

The implemented algorithm is the following set of sub functions:

1) Evaluation angle by arctangent of y/x ratio. The atan2(y,x) function is used,
2) The evaluation is executed only if exciter value is positive,
3) the value is multiplied by motor ***paipol*** to convert mechanical to electrical angle,
4) the compensation ***angofs*** is added to correct sensor alignment.

The compact formula is the following:

$$angle = \big(atan2(secsin, seccos)\big) * m2rppk + angofs$$

The ***m2rppk*** is motor pair poles divided by resolver pair poles.

Example: with motor pair poles = 6 and resolver pair poles = 2 the ***m2rppk*** shall be set to 6/2=2.

The function is executed only if valid inputs ***secsin***, ***seccos*** and ***priexc***.

The test for validity is the following:

$$\Big(\big(abs(secsin) + abs(seccos)\big) > C\_MINANV\Big)\ and\ (priexc \geq 0)$$

The evaluation of angle is executed at every ***start*** event when ***secsin*** and ***seccos*** reach the peak value to minimize evaluation error.

In between two evaluation events, the IP integrates motor speed at every ***start*** trigger.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 artix7 kintex7 virtex7 zynq	zynq	Xilinx FPGA Family name
C_MINANV	Integer	1..65535	8192	Minimum value for valid test in input values

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset the encoder. Active high.
m2rppk[16:0]	IN	Motor to Resolver Pair Poles ratio
angofs[31:0]	IN	Angle offset for alignment
speed [31:0]	IN	Motor electric speed
start	IN	Sync for interpolation
priexc[17:0]	IN	Resolver primary exciter. SIGNED18
secsin[17:0]	IN	Resolver secondary sine. SIGNED18
seccos[17:0]	IN	Resolver secondary cosine. SIGNED18
angle[31:0]	OUT	Phase electrical angle. UNSIGNED32. 2^{32}=360 degree

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the, Spartan 6 family and ZYNQ 7-family of FPGAs. The following tables lists the devices used for characterization using default IP parameters.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**ZYNQ**
Number of Slice Registers	337
Number of Slice LUTs	619
Number of fully used LUT-FF pairs	272
Number of Block RAM/FIFO	1
Number of DSP48E1s	2

Execution time

output	input	clock cycle[1]
angle[31:0]	start (evaluation angle)	36
angle[31:0]	start (integration)	1

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
14/02/2015	1.0	Initial QDeSys release
02/03/2015	1.1	QDeSys release
06/08/2017	1.2	Evaluation only on positive value of exciter
June 1, 2018	1.3	Rename paipol to m2rppk

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