FUNCTION

3-Level Pulse Frequency Modulation (PFM).

VHDL File

rpfm3phxlm.vhd

Applicable Devices

Spartan-3ADSP, Spartan 6, 7-Family

Xilinx primitive used

DSP48A
RAMB16_S18_S18

Sub modules used

Dsp4mot.vhd
bram1k18.vhd

Execution time

40 clock cycles

Introduction

This module implements a 3-level PFM modulator to control three-phase motors.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name
C_3_LEVEL	Integer	0,1	1	1=Enable 3-levels mode, 0=2-levels mode only
C_TPNC	Integer	0,1	1	1=TPNC gate unit mode, 0=NPC or default mode

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
modlevels[0:0]	IN	Requested modulation levels, UNSIGNED1: 0=2-levels, 1=3-levels
dc_link[16:0]	IN	Motor power supply voltage from the A/D. UNSIGNED17.
start	IN	Start calculation. Active high. The pulse width must be of 1 clock cycle.
angle[31:0]	IN	Required angle. UNSIGNED32.
modulo[16:0]	IN	Modulation value. UNSIGNED17.
modclkdv[7:0]	IN	Modulator clock divider. UNSIGNED8.
modpresc[3:0]	IN	Modulator prescaler. UNSIGNED4.
vec07nice	IN	Vector 0/7 nice transition.
vec7hold	IN	Vector 7 hold.
modzone[1:0]	OUT	Modulation mode/zone.
Inelabs	OUT	Computational engine working
inmodhs	OUT	High speed modulator working
finish	OUT	End of calculation. Computational engine finish work.
l2cdvx[2:0]	OUT	2-levels mode coil command output phase 3,2,1
l2sync	OUT	2-levels mode coil command sync event
l3cdv1[1:0]	OUT	3-levels mode coil command output phase-1
l3cdv2[1:0]	OUT	3-levels mode coil command output phase-2
l3cdv3[1:0]	OUT	3-levels mode coil command output phase-3
l3sync	OUT	3-levels mode coil command sync event

Detailed Description

The 3-levels RPFM modulator core works in the same way of 2-levels version of RPFM. Look to the 2-levels version datasheet for details.

The 3-levels version extends coil drive capability from 2^3=8 vector to 3^3=27 vectors.

The following table shows the vector set generated by modulator.
The vectors 0..7 are generated in both 2 and 3 levels modes.
The vectors 8..26 are generated in 3-levels mode only.

P3	*P2*	*P1*	*Vector Group*	*Vector number*	*Vector angle*	*Vector modulo*	*Description*
0	0	0	0	0	null	zero	All phases at same value: 0,1,2
1	1	1		7			
2	2	2		26			
0	0	2	1	1	0	2/3	Values 0,2 are used
0	2	2		2	60		
0	2	0		3	120		
2	2	0		4	180		
2	0	0		5	240		
2	0	2		6	300		
1	1	2	2	8	0	1/3	Values 1,2 are used
1	2	2		9	60		
1	2	1		10	120		
2	2	1		11	180		
2	1	1		12	240		
2	1	2		13	300		
0	0	1	3	14	0	1/3	Values 0,1 are used
0	1	1		15	60		
0	1	0		16	120		
1	1	0		17	180		
1	0	0		18	240		
1	0	1		19	300		
0	1	2	4	20	30	1/2	All three values used
0	2	1		21	90		
1	2	0		22	150		
2	1	0		23	210		
2	0	1		24	270		
1	0	2		25	330		

Table 1 - set of vectors

Vector 7 and 26 are available only if ***vec7nice***=1.

Vectors of group 2 and 3 are equivalent for the motor point of view.

Vectors of group 4 have 30 degrees offset comparing groups 1,2,3.

The active vectors are 24, 6 for active groups 1..4.
From the motor point of view the active vectors are 18 because the group “2” and group “3” are overlapped.

The following pictures shown the vectors.
The modulo of vectors correspond to relative current intensity.
The RED vectors are from group “1”,
The GREEN vectors are from group “2” and group “3 (overlapped),
The BLUE vectors are from group “4”.

Let assume the motor coils 1,2,3 are in position 0,120,240 degrees.

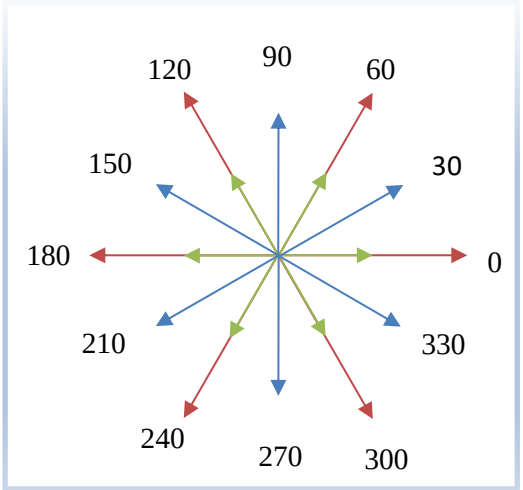

Figure 1 - current vectors to motor

TPNC option

In TPCN topology the “dc_link / 2” can be generated by a set of capacitor or batteries so:

- when vectors of group 2 are applied, the “dc_link/2” value move up to “dc_link” value and
- when vectors of group 3 are applied, the “dc_link/2” value move down to “zero” value.

To minimize this ripple effect the modulator can flip from group 2 to group 3 vectors and vice versa at every modulator output.

This feature can be enabled by setting C_TPNC=1.

Modulator pulse width

The modulator pulse width is generated according “modclkdv”, “modpresc” and “modlevels”.
The full description of modulator pulse width for 2-levels mode is described in QD_TDS_116.

When 3-levels mode is selected, the modulator works at half speed compared with 2-levels mode. The implementation correspond to expected behavior: 2-levels @ 3.2 uSec generate same ripple current of 3-levels @ 6.4 uSec.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	410
Number of Slice LUTs	744
Number of fully used LUT-FF pairs	286
Number of Block RAM/FIFO	1
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	20..28
l2sync	start	39
l3sync	start	40

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. Xilinx LogiCORE IP Block Memory Generator V6.1 [DS512 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
28/01/2015	1.0	QDeSys draft.
02/03/2015	1.1	QDeSys release.
20/12/2017	1.2	Update module signal interface

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