FUNCTION

Hall sensor

VHDL File

hallsnsp.vhd

Applicable Devices

Spartan3ADSP, Spartan6, Artix7, Kintex7, Virtex7, Zynq

Xilinx primitive used

RAM16X1D

Sub modules used

ram16xyd4m.vhd

Execution time

6..10 clocks

Introduction

The Hall sensor IP core provides elaboration for the raw signals received from hall sensors on the motor. The output is the electric angle. It is provided of a linear interpolation unit to generate intermediate values between consecutive hall commutation events. It operates in single 3 sensors or 6 sensors. The angle position is defined by the DPR registers.

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Detailed Description

The low cost hall sensors solution is largely used in BLDC motor for simple commutation six-steps control mode.

This module implements continuous angle value for the whole 360-degree rotation using the hall sensors commutation events to let FOC works in sinusoidal mode.

The IP is able to work with a single set of 3 hall sensors or with a double set of hall sensor.

The IP output is the motor electric angle in high-resolution format: 2^{32}=360 degrees (1~=83.82 nDeg)

The following table shows the 6-steps with angle correspondence and hall sensors levels. A double electric round is shows for better understanding the wrap between rounds.

Step	Angle	Phase-A	Phase-B	Phase-C
1	0	H	L	L
2	60	H	H	L
3	120	L	H	L
4	180	L	H	H
5	240	L	L	H
6	300	H	L	H
1	0	H	L	L
2	60	H	H	L
3	120	L	H	L
4	180	L	H	H
5	240	L	L	H
6	300	H	L	H

Figure 1 - the six steps

The 360-degree full electric round is divided in 6 steps of 60 degrees each, as consequence, the steps to angle function select a range.

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Step	Angle-min	Angle-center	Angle-max
1	330	0	30
2	30	60	90
3	90	120	150
4	150	180	210
5	210	240	270
6	270	300	330

Figure 2 - angle range for each step

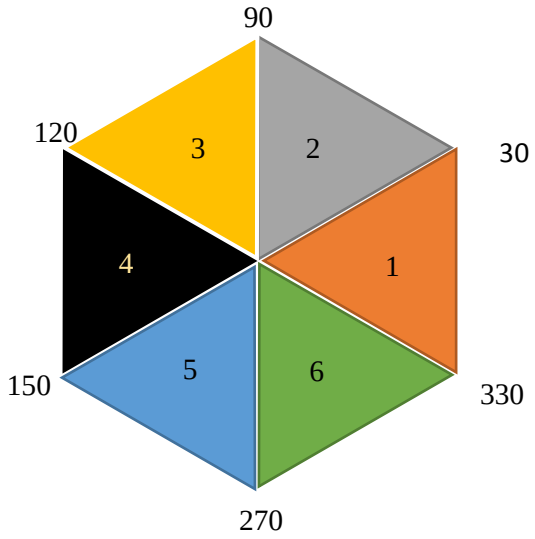

Figure 3 - the 6 sectors

The following diagram shown, on “Y” axe, the hall sensors digital levels. The sensors A,B and C corresponds to coil terminal of phases A,B and C.

On “X” axe the electric flux angle is displayed from -210 to 270 degrees in steps of 30 degrees.

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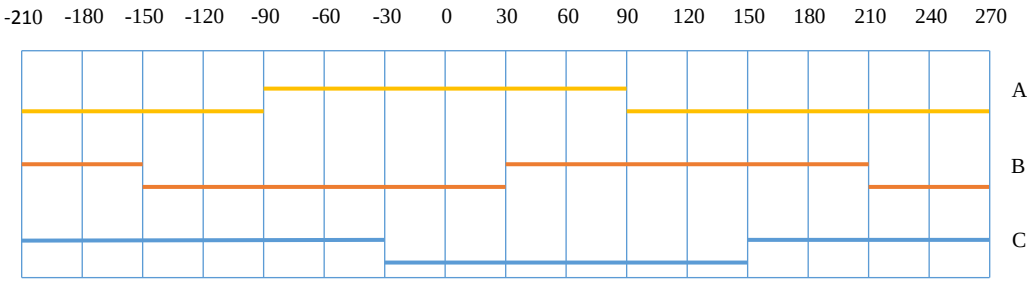

Figure 4 - phase sequence

In case of negative level on hall sensor digital signal, the phase is opposite or +/- 180 degrees.

FOC driving concept

In FOC a conventional PWM can be used to produce pseudo analog outputs with high resolution angles (not limited to six values). As consequence the phases A,B and C can be driven to produce any Is vectors (for both modulo and angles controlled by FOC).

$$phase_A = \cos\alpha$$

$$phase_B = \cos(\alpha - 120)$$

$$phase_C = \cos(\alpha - 240)$$

By convention, the main direction or forward direction is CCW because the angle increments correspond to anti clockwise rotation. As consequence the reverse direction is CW were angle decrements. The rotation refers to electric ***Vs*** vector were usually the motor rotor spin in CW direction.

Considering starting condition were driving motor winding at angle = 0° corresponding to step “1”.

If rotor is free to move (no load applied), the magnetic will align to winding of phase-A.

In order to drive the motor CCW we need to move **Is** phase over flux phase of 90° (in case of CW the angle shall be -90°).

The rotor start rotating CCW because ***Is*** is orthogonal to flux. When flux angle is 30° (angle-max of step “1”) the hall sensors detect angle 60°. This value correspond to 30° (angle-min of step “2”). The offset error is exactly -30°.

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The following table shows the angle relation between flux, and hall sensors.

Direction	Step	Angle hall sensor	Angle flux
stall	1..6	(Step-1)*60	(Step-1)*60
CCW	1..6	(Step-1)*60	(Step-1)*60-30
CW	1..6	(Step-1)*60	(Step-1)*60+30

In order to reduce the electric noise (and corresponding mechanical noise, vibration and power loss), a linear interpolation is used to generate intermediate angles between two consecutive steps.

The linear interpolation is always enabled: it starts at valid hall sensor signal changes and it stop after ***ctolim*** clocks.

ANGLE VALUES

The DPR is organized in 16 locations of 16 bits angle value.

The angle resolution is $360/2^{16}$ ~= $5.493*10^{-3}$ Deg

The following table shows the values used for first hall sensors set ***hallsig[2:0]***, add value 8 to address location for second hall sensors set ***hallsig[5:3]***.

Hallsig [2]	*Hallsig [1]*	*Hallsig [0]*	DPR ADDRESS	STEP	ANGLE VALUE	USAGE
-	-	-	0	-	-30	Forward Compensation
0	0	1	1	1	0	Angle for step 1
0	1	1	3	2	60	Angle for step 2
0	1	0	2	3	120	Angle for step 3
1	1	0	6	4	180	Angle for step 4
1	0	0	4	5	-120	Angle for step 5
1	0	1	5	6	-60	Angle for step 6
-	-	-	7	-	30	Backward Compensation

Figure 5 - memory format

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The forward compensation is applied when ***fwdir***=1 and ***moving***=1.

The backward compensation is applied when ***fwdir***=0 and ***moving***=1.

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PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 artix7 kintex7 virtex7 zynq	spartan3adsp	Xilinx FPGA Family name

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SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset the encoder. Active high.
mem_we	IN	Memory write enable
mem_addr[3:0]	IN	Memory address selector
mem_din[15:0]	IN	Memory data input
mem_dout[15:0]	OUT	Memory data output
ctolim[19:0]	IN	UNSIGNED20 timeout to costing mode
angtg	IN	Interpolator angle generation trigger
speed[31:0]	IN	Motor speed
fwdir	IN	1=Forward direction, 0=backward direction
moving	IN	1=moving, 0=stop
hallsig[5:0]	IN	Hall sensors
angle[31:0]	OUT	Phase electrical angle. UNSIGNED32. 2^{32}=360 degree
engev	OUT	Updated angle event

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TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation, Spartan 6 family and Kintex 7-family of FPGAs. The following tables lists the devices used for characterization using default IP parameters.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	139
Number of Slice Flip Flops	175
Number of 4 input LUTs	250

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	167
Number of Slice LUTs	220
Number of fully used LUT-FF pairs	137

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	166
Number of Slice LUTs	218
Number of fully used LUT-FF pairs	137

Execution time

output	input	clock cycle[1]
angle[31:0]	angtg	10
angle[31:0]	hallsig[5:0]	6

[1] Unless otherwise noted.

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Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
13/05/2014	1.0	Initial QDeSys release

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