

**Product Specification** 

## **FUNCTION**

Speed control loop IP.

#### **VHDL File**

spdcontrol.vhd

#### **Applicable Devices**

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

### Xilinx primitive used

DSP48A/A1/E1

## Sub modules used

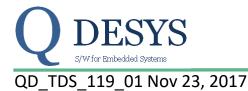
dsp4mot.vhd r32umlite.vhd

### **Execution time**

Parameters depend

## Introduction

This IP realizes the speed control loop with PI (Proportional Integral) regulator including with anti-windup control. The output is normalized avoid saturation, finaly a conversion to rectangular coordinates is applied



## **Detailed Description**

This module implements the speed loop using PI (Proportional Integral) regulator.

The generic PI formula is the following equation:

$$u_n = K_p e_n + K_i \frac{T}{T_i} \sum_{k=0}^n e_n$$

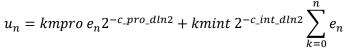
Equation 1: generic PI regulator

detailed

 $e_n = spdset - spdact$ Equation 2: the error

$$e_s = \sum_{k=0}^n e_n$$

#### Equation 3: error history



Equation 4: the IP core

 $u_{ns} = -outlim \le u_n \le outlim$ Equation 5: Saturation of PI result

> $outvlx = u_{ns} kmultx$  $outvly = u_{ns} kmulty$

Equation 6: signed modulo to vector rectangular

Where:



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 $u_n$  is the output value at the time n\*T  $e_n$  is the error at the time n\*T  $e_s$  is the sum of all errors  $K_p$  is the proportional gain  $K_i$  is the integrative gain  $T_i$  is the time constant of the integral

T is the sampling period

The calculation begins when the *start* signal is driven high for 1 clock cycle; the process terminates when the module sets the *finish* signal high for 1 clock cycle.

The set-point of the PI is the *spdset[31:0]* SIGNED32 argument and the feedback value is the *spdact[17:0]* SIGNED32 argument. The error is calculated as *spdset- spdact*.

The integrative accumulator is post increment of :  $e_n$ The anti-windup is implemented by post increment of :  $-e_n(c_indwp_kdiv + 2^{-c_indwp_dln2})$ 

The *kmpro[31:0]* BINARY32 (IEEE 754 32 bits floating point) argument is the multiplier of the proportional part of the PI module; referring to Error! Reference source not found. and Error! Reference source not found.

$$\frac{kmpro}{2^{c_pro_dln2}} = K_p$$

The *kmint[31:0]* BINARY32 (IEEE 754 32 bits floating point) argument is the multiplier of the integrator part of the regulator; referring to **Error! Reference source not found.** and to **Error! Reference source not found.** 

$$\frac{kmint}{2^{c\_int\_dln2}} = K_i\left(\frac{T}{T_i}\right)$$

The result of PI is saturated to ± *outlim[16:0]* UNSIGNED17.

Finally the *kmultx[17:0]* SIGNED18 is multiplied to produce output *outvalx[17:0]* SIGNED18, *kmulty[17:0]* SIGNED18 is multiplied to produce output *outvaly[17:0]* SIGNED18 and *finish* is asserted for just one clock .

The anti-windup is applied when saturation occur. In case of saturation the integrator is reduced by quantity proportional of last error.

$$e_s = e_s - (c_{indw_k div} + 2^{c_{indwp_d ln2}})e_r 2^{-c_{indp_d ln2}}$$



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## **PARAMETERS**

Parameter	Туре	Values	Default	Description
	string	spartan3adsp	zynq	Xilinx FPGA Family name
C_FAMILY		spartan6 kintex7		
C_PRO_DLN2	integer		1	Base 2 logarithm of proportional error divisor
	integer		5	Base 2 logarithm of integrative error divisor
	integer		1	Base 2 logarithm of integrative maximum error
C_INDWP_DLN2	Ū			for anti windup
C_INDWP_KDIV	integer		1	Integer maximum error for anti windup

#### **SIGNALS**

Signal	I/O	Description	
clock	IN	Clock (rising edge).	
reset	IN	Reset. Active high.	
start	IN	Start calculation. Active high. The pulse width must be of 1 clock cycle.	
spdset[31:0]	IN	Set point (SIGNED32) of the regulator.	
spdact[31:0]	0] IN Feedback value (SIGNED32) of the regulator.		
kmpro[31:0]	IN	Proportional gain of the regulator (BINARY32).	
kmint[31:0]	IN	Integral gain of the regulator (BINARY32).	
outlim[16:0]	IN	Output limiter (saturation value) (UNSIGNED17).	
kmultx[17:0]	IN	Output multiplier for X-coordinate (SIGNED18).	
kmulty[17:0]	IN	Output multiplier for Y-coordinate (SIGNED18).	
finish	OUT	Output available. Active high. The pulse width is of 1 clock cycle.	



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## TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

#### **Device Utilization**

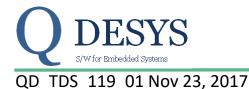
Device Utilization Summary (estimated values)		
Logic Utilization	ZYNQ	
Number of Slice Registers	534	
Number of Slice LUTs	1000	
Number of fully used LUT-FF pairs	420	
Number of DSP48E1s	1	

#### **Execution time**

output	input	clock cycles <sup>1</sup>
finish	start	146

<sup>&</sup>lt;sup>1</sup> Using default parameters.

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## **Reference Documents**

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

## **Support**

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

## **Ordering Information**

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

#### **Revision History**

Date	Version	Description
November 23, 2017	1.0	Initial QDeSys release

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