FUNCTION

Pulse Frequency Modulation (PFM).

VHDL File

rpfm3phmod.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A
RAMB16_S18_S18

Sub modules used

Dsp4mot.vhd
bram1k18.vhd

Execution time

39 clock cycles

Introduction

This module implements a PFM modulator to control three-phase motors.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
dc_link[16:0]	IN	Motor power supply voltage from the A/D. UNSIGNED17.
start	IN	Start calculation. Active high. The pulse width must be of 1 clock cycle.
angle[31:0]	IN	Required angle. UNSIGNED32.
modulo[16:0]	IN	Modulation value. UNSIGNED17.
modclkdv[7:0]	IN	Modulator clock divider. UNSIGNED8.
modpresc[3:0]	IN	Modulator prescaler. UNSIGNED4.
vec07nice	IN	Vector 0/7 nice transition.
vec7hold	IN	Vector 7 hold.
coildrv[2:0]	OUT	PFM coil driver signals.
modsync	OUT	Modulator synchronization output
modzone[1:0]	OUT	Modulation mode/zone.
Inelabs	OUT	Computational engine working
inmodhs	OUT	High speed modulator working
finish	OUT	End of calculation. Computational engine finish work.

Detailed Description

The RPFM modulator evaluate the *angle* and *modulo* of desired output Vs vector at each *start* trigger.
A programmable sigma delta modulator generates coils command at programmable rate. The minimum coil pulse width (low or high) is defined by *modclkdv* and *modpresc* signals.

The minimum pulse width time is:

$$Pwmin = Tclk * (modclkdv + 1) * (modpresc + 1)$$

Were *Tclk* is the main clock rate.

The high-speed *modclkdv* is used to divide the input *clock* rate. When the start signal is triggered, the counter is rounded to synchronize the modulator with the elaboration engine.

Example:
clock rate = 50 MHz, *Tclk* = 20 ns
desired Pwmin = 3.2 usec.
The clock divider shall be 3.2 us / 20 ns = 160
The right values are *modclkdv* = 9, *modpresc* = 15 ; (9 + 1) * (15 + 1) = 160

Pulse width in clocks	Modclkdv	Modpresc
30	1	14
38	18	1
39	2	12
4096	255	15

The absolute minimum pulse width is 30 clocks. Do not set values lower than this limit.

The pulse width in range 30 to 38 will produce jitter in coil command. These values can be used for high-speed modulation when the small jitter is acceptable.

The values from 39 and up may produce jitter if the *start* cycle (clocks between two consecutive start activations) is not divisible by the pulse width in clocks.

Pulse width in clocks	Start cycle in clocks	Jitter
40	160	No
40	161	Yes

The clock divisors *modclkdv* and *modpresc* can be changed on the fly. The new values are used after competition of modulation cycle.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**ZYNQ 7**
Number of Slice Registers	401
Number of Slice LUTs	724
Number of fully used LUT-FF pairs	249
Number of Block RAM/FIFO	1
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	20..28
modsync	start	39

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. Xilinx LogiCORE IP Block Memory Generator V6.1 [DS512 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
14/11/2011	1.0	QDeSys draft.
23/12/2011	1.1	Added parameters for FPGA family
10/07/2013	1.2	Description of pulse width programming
20/12/2017	1.3	Update module signal interface

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