FUNCTION

Cartesian coordinates to polar coordinates transformation.

VHDL File

rectopol.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A
RAMB16_S18_S18

Sub modules used

atan2.vhd
park.vhd

Execution time

61 clocks

Introduction

This module converts the (X, Y) Cartesian coordinates into the (M, θ) polar coordinates. The transformation is implemented using the following mathematical relation:

$$\begin{cases} \theta = \text{atan2}(\text{Y}, \text{X}) \\ M = X\cos\theta + Y\sin\theta \end{cases}$$

Equation 1: Cartesian to polar conversion

where:
X, Y are the Cartesian coordinate to convert
M is the radial coordinate in the polar system
θ is the angular coordinate in the polar system

Detailed Description

This IP core converts the (X, Y) Cartesian coordinates to the (M, θ) polar coordinates. The mathematical formula used to calculate the polar coordinates is Equation 1.

Equation 1	IP core parameter	Type	Note
X	***argX[17:0]***	SIGNED18	-
Y	***argY[17:0]***	SIGNED18	-
θ	***resP[19:0]***	UNSIGNED20	-
M	***resM[16:0]***	UNSIGNED17	-

The IP core uses the atan2 and the Park functions to execute the conversion. The angular coordinate θ is calculated applying the function atan2 to ***argX[17:0]*** and to ***argY[17:0]***; M is calculated applying the function Park to ***argX[17:0]***, ***argY[17:0]***, and ***resP[19:0]***.

The process begins when the ***start*** signal is set high for 1 clock cycle; the process terminates when the ***finish*** signal is set high for 1 clock cycle. The Cartesian coordinates to convert are the ***argX[17:0]*** and ***argY[17:0]*** SIGNED18 arguments. The output polar coordinates are the ***resP[19:0]*** UNSIGNED20 and the ***resM[16:0]*** UNSIGNED17 arguments. The first represents the θ angular coordinate; the second is the M radial coordinate. The angular coordinate ***resP[19:0]*** represents the normalized angle and the effective angle in degrees is:

$$\theta^{\circ} = \frac{resP[19:0]}{2^{20}} \cdot 360$$

The ***doneP*** flag indicates that the ***resP[19:0]*** data out is valid but doesn't indicate the end of the process. The ***finish*** signal is set high for 1 clock cycle at the end of the process and it indicates that both ***resP[19:0]*** and ***resM[16:0]*** data outputs are valid.

The ***reset*** signal resets the IP core and set all the outputs to 0. While reset is active (high) the ***start*** signal is ignored.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start command. It starts the process. Active high.
argX[17:0]	IN	X Cartesian coordinate. SIGNED18.
argY[17:0]	IN	Y Cartesian coordinate. SIGNED18.
resP[19:0]	OUT	θ angular coordinate. UNSIGNED20.
resM[16:0]	OUT	M radial coordinate. UNSIGNED17.
doneP	OUT	resP[19:0] data valid. Active high. The signal is driven high for 1 clock cycle when the resP[19:0] data out is valid.
finish	OUT	End of calculation. Active high. The signal is set high for 1 clock cycle at the end of the calculation and all the outputs (resP[19:0], resM[19:0]) are valid.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	278
Number of Slice Flip Flops	314
Number of 4 input LUTs	501
Number of BRAMs	2
Number of DSP48s	3

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	293
Number of Slice LUTs	369
Number of fully used LUT-FF pairs	235
Number of Block RAM/FIFO	2
Number of DSP48A1s	3

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	293
Number of Slice LUTs	451
Number of fully used LUT-FF pairs	235
Number of Block RAM/FIFO	2
Number of DSP48E1s	3

Execution time

output	input	clock cycle[1]
finish	start	61
doneP	start	43

[1] Unless otherwise noted.

Timing[2]

In the figure below there are the timings relative to a whole start/finish cycle of calculation.

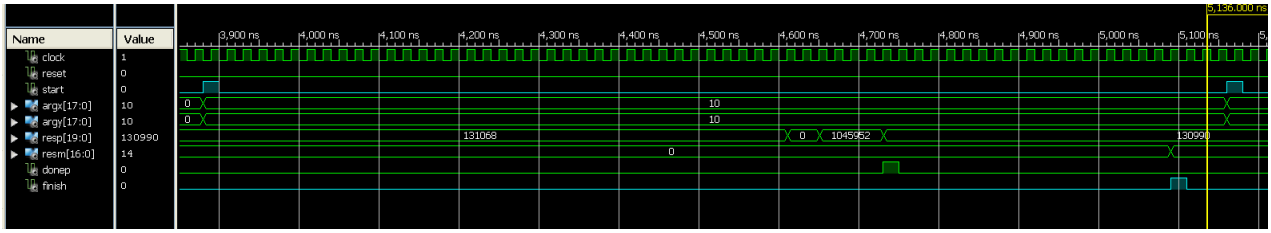

Figure 1: timings of a whole start/finish cycle

The process begins on the rising edge of the clock when the ***start*** signal is set high; all the inputs must be stable when ***start*** is set high (Figure 3) and they must stay stable until the ***finish*** signal is set high. The signal ***doneP*** is set high for 1 clock cycle when ***resP[19:0]*** is ready (Figure 2).

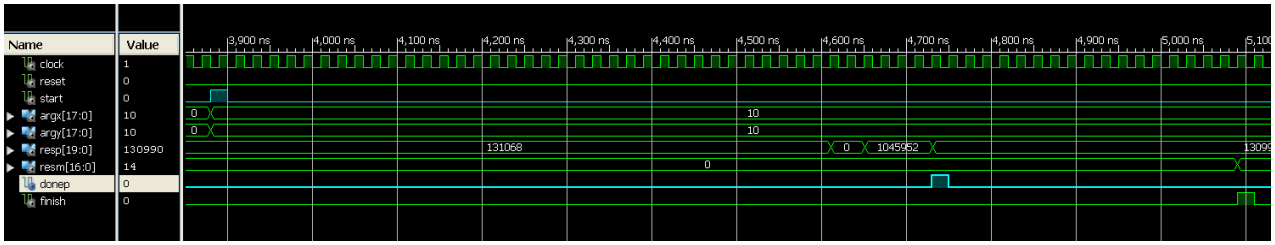

*Figure 2: timings of **start** and **doneP** signals*

Be aware that ***resM[16:0]*** is not ready when ***doneP*** is set high.

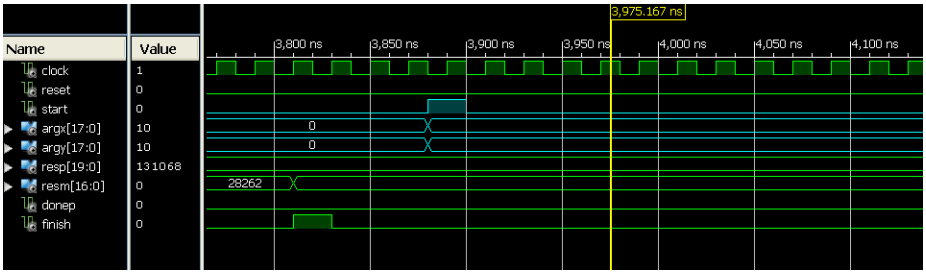

*Figure 3: timings of **start** and input signals*

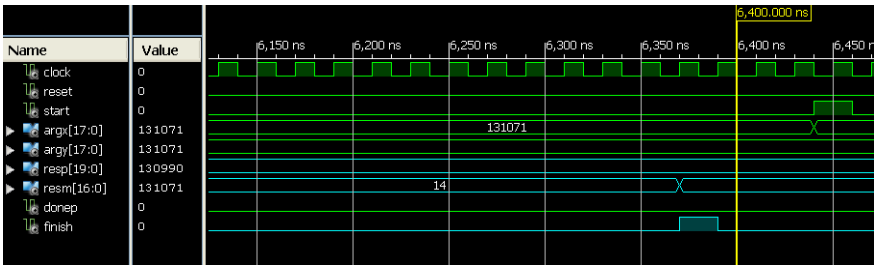

*Figure 4: timings of **finish** and output signals*

[2] The clock period is only chosen with the purpose to draw the waveforms.

The signal ***finish*** is set high for 1 clock cycle when the process terminates and the outputs ***resP[19:0]*** and ***resM[16:0]*** are valid. The outputs are valid until another ***start*** is sent to the process.

The ***reset*** signal, caught anytime on the rising edge of the clock, resets the core and sets the outputs to 0.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. Xilinx LogiCORE IP Block Memory Generator V6.1 [DS512 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
10/08/2011	1.0	QDeSys Initial release
22/12/2011	1.2	Added parameters for FPGA family
12/05/2012	1.3	Added Kintex 7 and Zynq support

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