FUNCTION

Sine and cosine functions.

File

sincos.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A
RAMB16_S18_S18

Sub modules used

bram1k18.vhd

Execution time

6 clock cycles

Introduction

The IP calculates the sine and cosine of an angle using a lookup table to speed up the calculation and doing a linear interpolation to improve the precision.

Detailed Description

This module calculates the sine or cosine function depending on the selection performed by the signal ***sinsel.*** If ***sinsel*** is set high (logical 1) the sine function is selected, otherwise the cosine function is selected.

sinsel	function calculated
low (logical 0)	cos(α)
high (logical 1)	sin(α)

The input angle ***angle[26:0]*** UNSIGNED27 represents an high resolution fixed point angle; the Equation 1 calculates the value of ***angle[26:0]*** given an angle α expressed in degrees.

$$\boldsymbol{angle}[\mathbf{26:0}] = \frac{2^{27} \cdot \alpha}{360}$$

Equation 1

The Equation 2 calculate the angle expressed in degrees given ***angle[26:0].***

$$\alpha = \frac{\boldsymbol{angle}[\mathbf{26:0}]}{2^{27}} \cdot 360$$

Equation 2

The signal ***resout[17:0]*** SIGNED18 is the result of the calculation; in Equation 3 there is the formula to transform the ***resout[17:0]*** signal in the mathematical value of sine or cosine (it depends by the value of ***sinsel*** signal) of the angle α.

$$outval = \frac{\boldsymbol{resout}[\mathbf{17:0}]}{2^{17}}$$

Equation 3

The process begins on the rising edge of the clock in which ***start*** goes high; the ***finish*** signal indicates the end of the process and the output data valid.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start sine/cosine calculation. The pulse width must be of 1 clock cycle.
sinsel	IN	Sine/cosine function selector (high= sine, low=cosine).
angle[26:0]	IN	Input angle (UNSIGEND27) expressed as $\frac{\alpha}{360} \cdot 2^{27}$ where α is the angle in degrees.
resout[17:0]	OUT	Output (SIGNED18) sine/cosine of angle. The value must be divided by 131072 to get the output value.
finish	OUT	End of calculation. The pulse width is 1 clock cycle.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	54
Number of Slice Flip Flops	71
Number of 4 input LUTs	47
Number of BRAMs	1
Number of DSP48s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	68
Number of Slice LUTs	74
Number of fully used LUT-FF pairs	67
Number of Block RAM/FIFO	1
Number of DSP48A1s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	67
Number of Slice LUTs	19
Number of fully used LUT-FF pairs	14
Number of Block RAM/FIFO	1
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	6

[1] Unless otherwise noted.

Timing[2]

In the figure below there are the timings relative to a whole start/finish cycle of calculation.

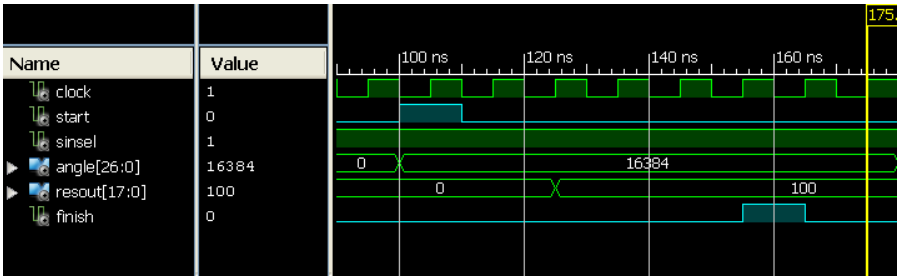

Figure 1: timings of a whole start/finish cycle

The process begins on the rising edge of the clock when the ***start*** signal is set high; all the inputs must be stable when the signal ***start*** is set high and they must stay stable until the signal ***finish*** is set high by the process.

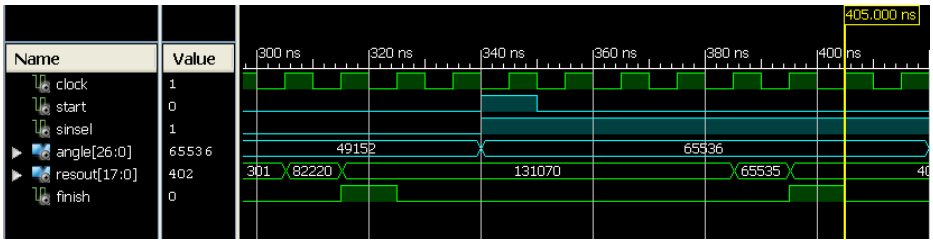

*Figure 2: timings of **start** and input signals **angle[26:0]** and **sinsel***

The output signal ***resout[17:0]*** is valid when the ***finish*** signal goes high and stays stable until a ***start*** signal or a ***reset*** is sent to the process.

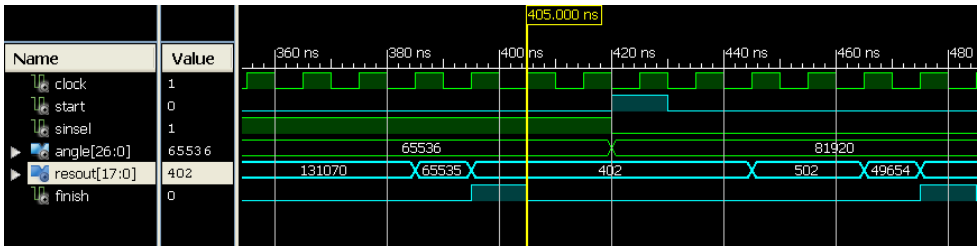

*Figure 3: timings for **finish** and **resout[17:0]***

The ***reset*** signal, caught anytime on the rising edge of the clock, resets the core and set ***resout[17:0]*** to 0.

[2] The clock period is only chosen with the purpose to draw the waveforms.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. Xilinx LogiCORE IP Block Memory Generator V6.1 [DS512 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
14/07/2011	1.0	Initial QDeSys release
22/12/2011	1.2	Added parameters for FPGA family
12/05/2012	1.3	Added Kintex 7 and Zynq support

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