FUNCTION

Low pass filter (first order).

File

filtiir.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A

Sub modules used

none

Execution time

4 clock cycles

Introduction

This block realizes a first order low pass filter. The differential equation that implements the low pass filter in the IP core is:

$$Y_j = Y_{j-1} + (X_j - Y_{j-1})K$$

Equation 1

Where:

Y_j is the output value calculate at the time $j \cdot T_s$

X_j is the input value at the time $j \cdot T_s$

K is a parameter to select the cutoff frequency

T_s is the sampling period of the input signal

Detailed Description

The IP core implements a first order low pass filter. The linear difference equation is the one in Equation 1. The Z-transform of the filter is

$$G(z) = \frac{Kz}{z + (K - 1)}$$

Equation 2: z-transform of the first order low pass filter implemented

The ***fktau[16:0]***UNSIGNED17 argument sets the value of K using the relation

$$K = \frac{\boldsymbol{fktau}[\mathbf{16}:\mathbf{0}]}{\mathbf{2^{17}}}$$

and so K is in the range of 0≤K<1.

The ***inraw[17:0]***SIGNED18 signal represents the input data; referring to Equation 1 it is the X_j term.

The ***outflt[17:0]***SIGNED18 is the output of the filter; referring to Equation 1 it is the Y_j term.

Filter setup considerations.

For a desired F_c in Hz (-3dB cutoff frequency of the filter) the relation

$$F_c = \frac{1}{2\pi\tau}$$

can be used to calculate the time constant τ of the filter.

$$\tau = \frac{1}{2\pi F_c}$$

Given the sampling time T_s we can define

$$T = \frac{1}{\left(e^{\frac{T_s}{\tau}} - 1\right)}$$

and finally

$$K = \frac{1}{(1 + T)}$$

Example:

If we want a cutoff frequency of F_c=25KHz with a sampling period of T_s= 3.2μsec, then:

τ=6.366*10^{-6}, T=1.531 and finally K = 0.395

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start of calculation pulse. The pulse width must be of 1 clock cycle. Active high.
fktau[16:0]	IN	Set K parameter of the filter. UNSIGNED17
inraw[17:0]	IN	Input data of the filter. SIGNED18.
outflt[17:0]	OUT	Filter data output. SIGNED18.
finish	OUT	End of calculation pulse. The pulse width is of 1 clock. Active high.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	25
Number of Slice Flip Flops	27
Number of 4 input LUTs	44
Number of DSP48s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	24
Number of Slice LUTs	26
Number of fully used LUT-FF pairs	24
Number of DSP48A1s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	23
Number of Slice LUTs	62
Number of fully used LUT-FF pairs	22
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	4

[1] Unless otherwise noted.

Timing[2]

In the figure below there are the timings relative to a whole start/finish cycle of the process.

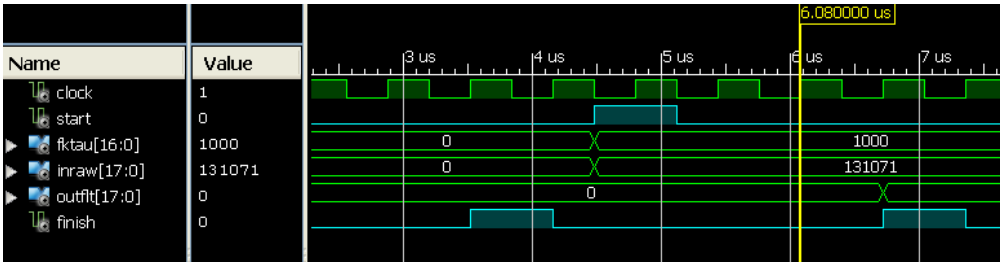

*Figure 1: timings of a whole **start**/**finish** cycle*

The process begins on the rising edge of the clock when the ***start*** signal is set high; the ***fktau[16:0]*** and ***inraw[17:0]*** input signals must be stable at this point and they must stay stable until the ***finish*** signal is set high by the process (see Figure 2).

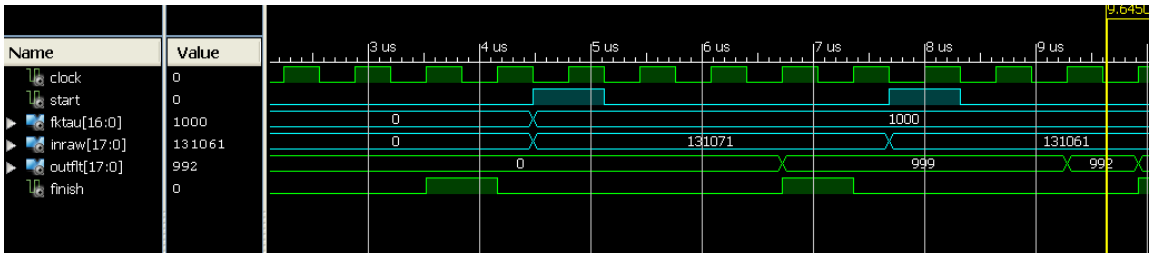

*Figure 2: timings of **start** and input signals*

The ***finish*** signal is set high for 1 clock cycle when the process terminates and ***outflt[17:0]*** is valid. The ***outflt[17:0]*** signal is valid until another ***start*** signal is set high or a ***reset*** is received by the process.

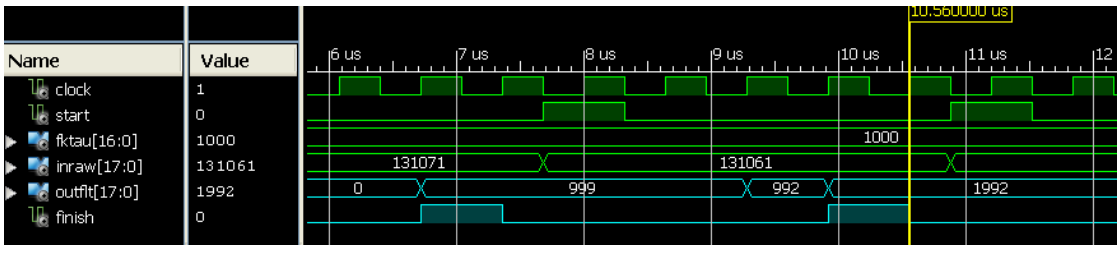

*Figure 3: timings for **finish** and **outflt[17:0]** signals*

The ***reset*** signal, caught anytime on the rising edge of the clock, resets the core and set ***outflt[17:0]*** to 0.

[2] The clock period is only chosen with the purpose to draw the waveforms.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

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Revision History

Date	Version	Description
15/07/2011	1.0	Initial QDeSys release.
22/12/2011	1.2	Added parameters for FPGA family
12/05/2012	1.3	Added Kintex 7 and Zynq support

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