FUNCTION

Clarke's transformation

VHDL File

clarke.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A

Sub modules used

none

Execution time

0,6,9 clocks

Introduction

This IP implements a Clarke's transformation. It converts a three-phase currents system (I_a, I_b, I_c) to a two-phase orthogonal system (I_α, I_β). Given the three currents I_a, I_b, I_c with $I_a+I_b+I_c=0$ and considering I_α overlapped to I_a the transformation is:

$$\begin{cases} I_\alpha = I_a \\ I_\beta = \frac{1}{\sqrt{3}} I_a + \frac{2}{\sqrt{3}} I_b \\ I_a + I_b + I_c = 0 \end{cases}$$

Equation 1

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Detailed Description

The Clarke's transformation is used to convert the three 120 degrees currents of three-phase motors to the equivalent two 90 degrees currents of bipolar motors. The mathematical transformation is described by the Equation 1.

In the practical use we consider two main cases:

- Stepper motors. Consist of a two phase system. The angle between the two phases is 90 degrees. We have two coil drivers and two current sensors. In this case the Clarke's transformation is not required for the motor control.
- Three-phases motors using 2-phases. The angles between the phases are 120 degrees. We have three coil drivers and two current sensors (the third current sensor is not needed because $I_a+I_b+I_c=0$).
- Three-phases motors using 3-phases. This implementation works with all 3-phases.

The input arguments ***inA[17:0], inB[17:0]*** and ***inC[17:0]*** are defined as SIGNED18 values and the valid range is -131072 … 131071. The value inC is used only in MODE 3.

The output results ***outX[17:0]*** and ***outY[17:0]*** are defined as SIGNED18 values and the valid range is -131072..131071.

The execution of the process is controlled by the ***start*** command; the ***finish*** signal is set high for 1 clock cycle at the end of the conversion and the outputs are ready.

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PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name
C_CLARKE_NPHS	integer	0..3	3	0=2-phases system 2=3-phases system, use only 2-phases 3=3-phases system, full implementation

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start command. It must be a pulse of 1 clock cycle. Active high.
inA[17:0]	IN	I_a input phase of a three-phase current system.
inB[17:0]	IN	I_b input phase of a three-phase current system.
inC[17:0]	IN	I_c input phase of a three-phase current system.
outX[17:0]	OUT	I_α output phase of the two-phase current system.
outY[17:0]	OUT	I_β output phase of the two-phase current system.
finish	OUT	End of calculation. Active high. The pulse width is of 1 clock cycle.

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TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	69
Number of Slice LUTs	98
Number of fully used LUT-FF pairs	49
Number of DSP48E1s	1

Execution time

output	input	clock cycle[1]
Finish	start	0=transparent 6=2-phases 9=3-phases

[1] Unless otherwise noted.

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Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
10/08/2011	1.0	QDeSys Initial release
18/11/2011	1.1	Modified Devices utilization table
22/12/2011	1.2	Added parameters for FPGA family
12/05/2012	1.3	Added Kintex 7 and Zynq support.
19/05/2016	1.4	Extend to 3-phases evaluation.

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