FUNCTION

Resolver sensor

VHDL File

resolver.vhd

Applicable Devices

Spartan3ADSP, Spartan6, 7-family, UltraScale+

Xilinx primitive used

-

Sub modules used

atan2.vhd
dsp48a4m.vhd

Execution time

66 cycles

Introduction

The Resolver sensor IP core provides elaboration for the analog data acquired from resolver sensor. The output is the electric angle, resolver angle and resolver speed. It is provided of a linear interpolation unit to generate intermediate values between consecutive valid evaluations.

Detailed Description

The resolver IP support two and three analog inputs resolver.

Digital filters are used to smoot evaluated angle and speed.

A LUT (look up table) can be used to linearize the sensor.

Check on exciter signal

The test for strong exciter signal is implemented by following code:

$$excstrong = abs(priexc) > C\_EXCMIN$$

The exciter shall change the polarity (MSB) before time C_EXCTMO (activation units).

In case of timeout or weak signal the exciter is considered stuck or not implemented and the resolver IP decode the angle using only SIN and COS inputs only.

Check on SIN/COS input

A minimum magnitude of SIN/COS input is required to enable the new angle evaluation.

The test for validity is the following:

$$socstrong = \Big(\big(abs(secsin) + abs(seccos)\big) > C\_SOCMIN\Big)$$

If weak magnitude the angle evaluation continues in coasting mode by integration of evaluated speed.

The motor to resolver pole pairs ratio is used in electric angle evaluation to let usage motor with different pole pairs number.

An angle offset correction is implemented to correct the alignment between resolver sensor and motor magnetic flux.

A double LPF digital filter is used to evaluate the resolver speed.

A double LPF digital filter is used to filter the resolver angle.

Angle correction LUT

A programmable LUT is implemented to correct nonlinear response of resolver and h/w interface.

The LUT usage is defined by following table

Mode	C_ANGLUT	LUT entries
disabled	0	0
enabled	1..3	$2^{C\_ANGLUT+9}$

When LUT is enabled, we have two working methods.

Mode	C_ALRELK	description
Absolute	255	LUT entry is resolver angle
Relative	0..18	LUT entry is added to resolver angle

Resolver angle evaluation

The compact formula is the following:

$$mangle = \big(atan2(secsin, seccos)\big)$$

$$eangle = mangle * m2rppk + angofs$$

The *mangle* can be optionally correct with LUT.

In case of invalid SIN/COS the *mangle* is evaluated by integration of evaluated speed.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 artix7 kintex7 virtex7 zynq zynquplus	zynq	Xilinx FPGA Family name
C_EXCMIN	Integer	-	50000	Minimum value for |EXC| input values
C_SOCMIN	Integer	-	50000	Minimum value for |SIN|+|COS| input values
C_EXCTMO	Integer	-	100	Exciter timeout
C_EXCPOL	Integer	0..2	0	Exciter polarity 0=both, 1=positive, 2=negative
C_ANGLUT	Integer	0..3	-	Angle correction LUT. 0=disabled, 1=1024 entries 2=2048 entries 3=4096 entries
C_ANGFLT	Integer	0..1	0	Angle digital filter 0=disabled, 1=enabled
C_ALRELK	Integer	-	5	LUT angle correction mode 0..18=relative mode 255=absolute mode

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset the encoder. Active high.
		Angle LUT DPR access host side
mem_en	IN	Access enables
mem_we	IN	Write enable 0=read only, 1=write enable
mem_addr[31:0]	IN	Address
mem_din[17:0]	IN	Write data input
mem_dout[17:0]	OUT	Read data output
start	IN	Elaboration Sync trigger: expected fixed rate
m2rppk[16:0]	IN	Motor to Resolver Pair Poles ratio
angofs[31:0]	IN	Angle offset for alignment
spdkft[16:0]	IN	Speed LPF filter K=value*2^{-17}
angkft[16:0]	IN	Angle LPF filter K=value*2^{-17}
priexc[17:0]	IN	Resolver primary exciter. SIGNED18
secsin[17:0]	IN	Resolver secondary sine. SIGNED18
seccos[17:0]	IN	Resolver secondary cosine. SIGNED18
eangle[31:0]	OUT	Phase electrical angle. UNSIGNED32. 2^{32}=360 degree
mangle[31:0]	OUT	Resolver angle
mspeed[31:0]	OUT	Resolver speed
finish	OUT	End of processing

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device ZYNQ 7-family of FPGAs. The following tables lists the devices used for characterization using default IP parameters.

Execution time

output	input	clock cycle[1]
finish	start (evaluation angle)	66

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
14/02/2015	1.0	Initial QDeSys release
02/03/2015	1.1	QDeSys release
06/08/2017	1.2	Evaluation only on positive value of exciter
June 1, 2018	1.3	Rename paipol to m2rppk
April 12, 2022	1.4	Angle LUT and digital filters

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