FUNCTION
Position estimator for sensorless motor control.

VHDL File
posslmeval.vhd

Applicable Devices
Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used
DSP48A/A1/E1
RAM16X1D

Sub modules used
dsp4mot.vhd
rectopol.vhd
ram16xyd4m.vhd

Execution time
128 clocks

Introduction
This module realizes the position estimator for a sensor less motor control. The state observer is realized using a sliding mode control algorithm that estimates the back-EMF vector and then the electrical rotor position.

Detailed Description

The electrical rotor position evaluation in the SFOC (Sensor less Field Oriented Control) is performed using a sliding mode control algorithm. It takes as input the two measured currents of the motor and uses a model of the motor itself to estimate the electrical rotor angle. The current vector estimated is compared with the real measured current vector and the result is used to adjust the motor model algorithm. Below is reported the equation in the continuous time domain used in the motor model.

$$v_s = Ri_s + L\frac{di_s}{dt} + e_s$$

Equation 1: motor model

where:
v_s is the input voltage vector
i_s is the motor current vector
e_s is the back EMF vector
R is the winding resistance
L is the winding inductance

If **usevsact**=0 the Vs target (**vs_set**) values is used else the Vs measured (**vs_act**) is used.

Solving Equation 1 for i_s in the discrete domain:

$$i_s(n+1) = \left(1 - T_s\frac{R}{L}\right)i_s(n) + \frac{T_s}{L}(v_s(n) - e_s(n))$$

Equation 2: current vector in the discrete domain

where:
T_s is the sampling time
$i_s(n+1)$ is the current at the $(n+1)*T_s$ time

The state observer uses the equation below to calculate and compensate the estimated current:

$$i_s(n+1) = \left(1 - T_s\frac{R}{L}\right)i_s(n) + \frac{T_s}{L}(v_s(n) - e_s(n) - z_s)$$

Equation 3: estimated current vector

The back-EMF correction vector used in the sliding mode controller is $\mathbf{z_s}$ and it is calculated as

$$z_s = \frac{vs\_mult * (v_s - e_s - z_s) - is\_mult * i_s}{2^{C\_ZS\_KDIV\_LN2}}$$

Equation 4: back-EMF correction vector

The $\boldsymbol{z_s}$ is limited by ***zs_max*** signal to $|z_s| \le zs\_max$.
The $\boldsymbol{e_s}$ vector is evaluated applying a Low Pass Filter (LPF1) to the $\boldsymbol{z_s}$ vector:

$$e_s = LPF1(z_s, es1\_kflt)$$

The ***bemf*** vector is evaluated applying a LPF1 to the $\mathbf{e_s}$ vector:

$$bemf = LPF1(e_s, es2\_kflt)$$

The parameter es2_kflt is evaluated dynamically using the equation reported below:

$$es2\_kflt = es2\_kfmx \cdot \frac{|speed|}{2^{C\_F2\_KDIV\_LN2}} + es2\_kflo$$

where:
es2_kfmx is a multiplier
speed is the evaluated speed value
C_F2_KDIV_LN2 is a constant
es2_kflo is the value of es2_kflt when speed=0

The ***bemf_m*** (back-EMF modulo) and ***bemf_p*** (back-EMF angle) are evaluated by the rec2pol[1] function applied to ***bemf_x*** and ***bemf_y***:

$$bemf\_p = atan2(bemf\_y, bemf\_x)$$
$$bemf\_m = \sqrt{bemf\_x^2 + bemf\_y^2}$$

Equation 5: back-EMF angle and module

where:
bemf_m is the back-EMF module in polar coordinate
bemf_p is the back-EMF angle in polar coordinate
bemf_x is the back-EMF X component in Cartesian coordinate
bemf_y is the back-EMF Y component in Cartesian coordinate

The rotor angle ***bemf_p*** is corrected using a correction angle ***angofs***. The 16-bits are signed extended to 32bit value before sum.
The electrical rotor angle is:

$$angle = bemf\_p + angofs$$

Equation 6: estimated electrical rotor angle

where:
angle is the estimated electrical rotor position angle
bemf_p is the estimated electrical angle without correction
ang_adj is the correction angle calculated using the look-up table

In Figure 1 there is the diagram of the operations executed by the position estimator.

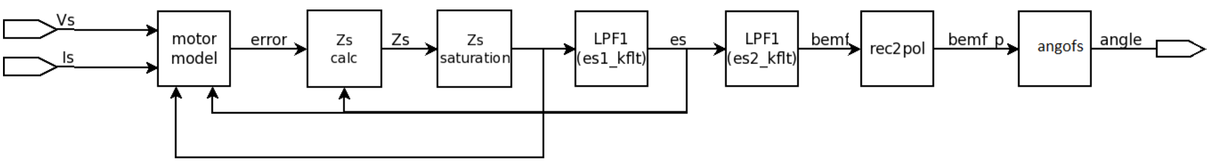

Figure 1: position estimator

[1] see QD_TDS_112_01 document for more details

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	zynq	Xilinx FPGA Family name
C_ZS_DLN2	integer	22..26	24	Base 2 logarithm of proportional error divisor
C_F2_DLN2	integer	26..30	28	Base 2 logarithm divider use to eval K of 2^{nd} LPF

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start calculation. Active high. The pulse width must be of 1 clock cycle.
angdef[31:0]	IN	Default angle.
rstang	IN	Reset angle.
usevsact	IN	Use Vs measured instead of Vs target
vs_mult[31:0]	IN	UNSIGNED32 Vs multiplier for slide mode function.
is_mult[31:0]	IN	UNSIGNED32 Is multiplier for slide mode function.
zs_max[16:0]	IN	UNSIGNED17 Zs clipping value for big-bang correction
es1_kflt[16:0]	IN	UNSIGNED17. K parameter of the LPFT1 pos eval BEMF1.
es2_kflo[16:0]	IN	UNSIGNED17. K parameter of the LPFT1 pos eval BEMF2 K @ speed=0
es2_kfmx[16:0]	IN	UNSIGNED17. Speed to K multiplier to evaluate K of the LPFT1 pos eval BEMF2.
es2_kflt[16:0]	OUT	UNSIGNED17. K parameter of the LPFT1 pos eval BEMF2.
angofs[15:0]	IN	SIGNED16 angle offset / 65536 for offset compensation
speed[31:0]	IN	SIGNED32, speed value; 2^{32} is full round in time unit
vs_set_x[17:0]	IN	SIGNED18, Vs X component (target value)
vs_set_y[17:0]	IN	SIGNED18, Vs Y component (target value)
vs_act_x[17:0]	IN	SIGNED18, Vs X component (measured value)
vs_act_y[17:0]	IN	SIGNED18, Vs Y component (measured value)
is_set_x[17:0]	IN	SIGNED18, Is X component (target value)
is_set_y[17:0]	IN	SIGNED18, Is Y component (target value)
is_act_x[17:0]	IN	SIGNED18, Is X component (measured value)
is_act_y[17:0]	IN	SIGNED18, Is Y component (measured value)
bemf_x[17:0]	OUT	SIGNED18. Bemf X.
bemf_y[17:0]	OUT	SIGNED18. Bemf Y.

bemf_p[31:0]	OUT	UNSIGNED31. Bemf vector angle.
bemf_m[16:0]	OUT	UNSIGNED17. Bemf vector modulo.
angle[31:0]	OUT	UNSIGNED31. Rotor position angle.
finish	OUT	End of calculation. Active high. The pulse width is of 1 clock cycle.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3, Spartan 6 and Kintex 7 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	603
Number of Slice LUTs	883
Number of fully used LUT-FF pairs	345
Number of Block RAM/FIFO	1
Number of DSP48E1s	4

Execution time

output	input	clock cycles[2]
finish	start	113

[2] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. QD_TDS_112_01 [rectopol specification, QDESYS 2012]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.
QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
14/11/2011	1.0	QDeSys draft.
22/03/2012	1.1	QDeSys release
12/05/2012	1.2	Added position estimator diagram.
5-Jan-17	1.3	Single value for angle offset compensation.
27-Jun-19	1.4	Update with Vs measured
6-Sep-19	1.5	Correct angle offset compensation reference

Disclaimer