

FUNCTION

System registers and interfaces for motor Field Oriented Control (FOC).

VHDL File

mosysfoc.vhd

Applicable Devices

Spartan3ADSP, Spartan6, 7-Family, UltraScale+

Xilinx primitive used

DSP48A/A1/E1

RAMB16_S18_S18

Sub modules used

motorfoc.vhd

Execution time

-

Introduction

This module is an interface toward the system registers of the motorfoc (motor Field Oriented Control) module. It implements the addressing of the registers and the read and write process.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 artix7 kintex7 virtex7 zynq	zynq	Xilinx FPGA Family name
Inverter analog inputs				
C_INV_IN_MAP[11:0]	Std_logic_vector	0x000..0xFFFF	0x083	Bit map enabled input channels: 0=IPHS_A 1=IPHS_B 2=IPHS_C 3=IBUS_X 4=VPHS_A 5=VPHS_B 6=VPHS_C 7=VBUS_X 8=VPHS_N
C_INV_IN_NOT[11:0]	Std_logic_vector	0..511	0x000	Bit map inverted channels. Bit values as per C_INV_IN_MAP
C_INV_OFSV_MODE	Integer	0..3	1	Offset set mode functions bit definition: 0=Self-Zero 1=S/W registers
C_INV_OVER_IPHS	integer	0..1	1	Overcurrent detection motor phases
C_INV_OVER_IBUS	integer	0..1	1	Overcurrent detection dc_link
C_INV_FILTER	Integer	0..1	1	2nd order LPF inputs
C_CLARKE_NPHS	Integer	0,2,3	3	Clarke transform input phases. 0=transparent (2-phases only for bipolar stepper motor) 2=2-phases used in 3-phases motor 3=3-phases used in 3-phases motor

C_PWM_MODULATOR	integer	0..2	1	Include PWM modulator IP
C_RPFM_MODULATOR	integer	0..2	1	Include RPFM modulator IP
C_RPFM_3_LEVEL	integer	0..1	1	RPFM 3-level extension
C_RPFM_TPNC	integer	0..1	1	RPFM 3-level T-PNC variant
C_SMO_EVAL	integer	0..1	1	Include SMO Position Estimator IP
C_SPD_EVAL	integer	0..1	1	Include Speed Measurement IP
C_SPEED_CTRL	Integer	0..1	1	Include speed loop
C_RESOLVER	integer	0..1	1	Include resolver sensor IP
C_RSV_MINANV	integer	1..65536	8192	Resolver Minimum Input Values
C_HALLSENSOR	integer	0..1	1	Include hall sensor IP
C_ENCODER	Integer	0..1	2	Include enhanced 2..3 wire encoder IP
C_MANROT	Integer	0..2	2	Scalar mode rotor angle IP: 0=no, 1=angle update, 2=enhanced with ramp and 2 nd order filter
C_MRT_ACCMAX_DLN2	Integer	8..16	16	Base 2 logarithm of MRT acceleration limiter
C_SMO_ZS_DLN2	integer	22..26	24	Base 2 logarithm of proportional error divisor
C_SMO_F2_DLN2	integer	26..30	28	Base 2 logarithm divider use to eval K of 2 nd LPF
C_SLP_PRO_DLN2	Integer	0..n	1	Base 2 logarithm of speed loop proportion error regulator

C_SLP_INT_DLN2	Integer	0..n	5	Base 2 logarithm of speed loop integrative error regulator
C_SLP_INDWP_DLN2	Integer	0..n	1	Base 2 logarithm of speed loop integrative error regulator for anti windup
C_SLP_INDWP_KDIV	Integer	0..n	1	Base 2 logarithm of speed loop integrative error regulator for anti windup
C_ISOVERFLOW_CMAX	integer	1..15	1	Current modulo overflow counter limit
C_PI_ERPRO_DLN2	integer	0..n	12	Base 2 logarithm of current loop PI proportional error divisor
C_PI_ERINT_DLN2	integer	0..n	18	Base 2 logarithm of current loop PI integrative error divisor

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
host_en	IN	Host access enable. Active high.
host_we	IN	Host write access enable. Active high.
host_addr[31:0]	IN	Host memory address.
host_din[31:0]	IN	Host data bus write word32
host_dout[31:0]	OUT	Host data read word32
host_ack	OUT	Host data transfer acknowledge
ext_angle[31:0]	IN	External rotor position sensor interface
Analog resolver sensor inputs for position evaluation (see QD_TDS_124 for description)		
rsv_priexc[17:0]	IN	Resolver primary winding exciter
rsv_secsin[17:0]	IN	Resolver secondary winding sine
rsv_seccos[17:0]	IN	Resolver secondary winding cosine
Hall sensor digital signals position evaluation (see QD_TDS_122 for description)		
hls_hallsig[5:0]	IN	Hall sensors digital inputs
Encoder position evaluation (see QD_TDS_101 for more details)		
enc_cha	IN	Encoder channel A.
enc_chb	IN	Encoder channel B.
enc_chi	IN	Encoder channel index.
Inverter analog, values are SIGNED18.		
acq_iphs_a[17:0]	IN	Motor current Phase-A
acq_iphs_b[17:0]	IN	Motor current Phase-B
acq_iphs_c[17:0]	IN	Motor current Phase-C
acq_ibus_x[17:0]	IN	Dc_link current
acq_vphs_a[17:0]	IN	Motor voltage Phase-A
acq_vphs_b[17:0]	IN	Motor voltage Phase-B
acq_vphs_c[17:0]	IN	Motor voltage Phase-C
acq_vbus_x[17:0]	IN	Dc_link voltage
acq_sync	IN	Acquisition synchronization.
Inverter analog offset, values are SIGNED18.		
ofs_iphs_a[17:0]	OUT	Motor current Phase-A
ofs_iphs_b[17:0]	OUT	Motor current Phase-B
ofs_iphs_c[17:0]	OUT	Motor current Phase-C
ofs_ibus_x[17:0]	OUT	Dc_link current

ofs_vphs_a[17:0]	OUT	Motor voltage Phase-A
ofs_vphs_b[17:0]	OUT	Motor voltage Phase-B
ofs_vphs_c[17:0]	OUT	Motor voltage Phase-C
ofs_vbus_x[17:0]	OUT	Dc_link voltage
Inverter analog normalized, values are SIGNED18.		
nrm_iphs_a[17:0]	OUT	Motor current Phase-A
nrm_iphs_b[17:0]	OUT	Motor current Phase-B
nrm_iphs_c[17:0]	OUT	Motor current Phase-C
nrm_ibus_x[17:0]	OUT	Dc_link current
nrm_vphs_a[17:0]	OUT	Motor voltage Phase-A
nrm_vphs_b[17:0]	OUT	Motor voltage Phase-B
nrm_vphs_c[17:0]	OUT	Motor voltage Phase-C
nrm_vbus_x[17:0]	OUT	Dc_link voltage
nrm_sync	OUT	Data synchronization.
Inverter analog filtered, values are SIGNED18.		
flt_iphs_a[17:0]	OUT	Motor current Phase-A
flt_iphs_b[17:0]	OUT	Motor current Phase-B
flt_iphs_c[17:0]	OUT	Motor current Phase-C
flt_ibus_x[17:0]	OUT	Dc_link current
flt_vphs_a[17:0]	OUT	Motor voltage Phase-A
flt_vphs_b[17:0]	OUT	Motor voltage Phase-B
flt_vphs_c[17:0]	OUT	Motor voltage Phase-C
flt_vbus_x[17:0]	OUT	Dc_link voltage
flt_sync	OUT	Data synchronization.
ovi_iphs_a	Out	Motor Phase-A overcurrent
ovi_iphs_b	Out	Motor Phase-B overcurrent
ovi_iphs_c	Out	Motor Phase-C overcurrent
ovi_ibus_x	Out	DC_link overcurrent
ismodover	Out	Is modulo overcurrent
generator	IN	0=drive mode, 1=generator mode
modtype[0:0]	IN	Selected modulator 0=PWM, 1=RPFM
modlevels[0:0]	IN	Modulator levels 0=2-levels, 1=3-levels
is3phases	IN	Three-phase motor selection flag. Active high ("1").
PWM 2-phases, 2-levels output		
pwm2p_l2c1w1 [1:0]	OUT	coil-1, winding-1
pwm2p_l2c2w1 [1:0]	OUT	coil-2, winding-1
pwm2p_l2c1w2 [1:0]	OUT	coil-1, winding-2
pwm2p_l2c2w2 [1:0]	OUT	coil-2, winding-2

pwm2p_l2sync	OUT	Sync signal
PWM 3-phases, 2-levels output		
pwm3p_l2cxw1 [2:0]	OUT	Coil 321, winding-1
pwm3p_l2cxw2 [2:0]	OUT	Coil 321, winding-2
pwm3p_l2sync	OUT	Sync signal
RPFM 3-phases, 2-levels output		
rpfm3p_l2cxw1 [2:0]	OUT	Coil 321, winding-1
rpfm3p_l2cxw2 [2:0]	OUT	Coil 321, winding-2
rpfm3p_l2sync	OUT	Sync signal
RPFM 3-phases, 3-levels output		
rpfm3p_l3c1w1[1:0]	OUT	Coil1, winding-1
rpfm3p_l3c2w1[1:0]	OUT	Coil2, winding-1
rpfm3p_l3c3w1[1:0]	OUT	Coil3, winding-1
rpfm3p_l3c1w2[1:0]	OUT	Coil1, winding-2
rpfm3p_l3c2w2[1:0]	OUT	Coil2, winding-2
rpfm3p_l3c3w2[1:0]	OUT	Coil3, winding-2
rpfm3p_l3sync	OUT	Sync signal
Deadtval[7:0]	Out	UNSIGNED8 gate unit dead time valid code
Gswcnt[31:0]	IN	UNSIGNED32, gate unit switches diagnostic counter
Hwfail	IN	Gate unit h/w failure
Hwkill	IN	Gate unit KILL input (fast cut-off)
coilgear	OUT	Coil signal gear
coilenab	OUT	Coil signals enable
syserr	OUT	Motor control IP system error
reseterr	OUT	Reset latched errors
zerocurr	OUT	Zero current offset
zerovbusx	Out	Zero DC_link offset command
zerovphsx	Out	Zero motor phases command
Scope / probe signals		
pix_setval[17:0]	OUT	SIGNED18. Current control probe X-set
piy_setval[17:0]	OUT	SIGNED18. Current control probe Y-set
pix_fb kval[17:0]	OUT	SIGNED18. Current control probe X-feedback
piy_fb kval[17:0]	OUT	SIGNED18. Current control probe Y-feedback
pix_outval[17:0]	OUT	SIGNED18. Current control probe X-output
piy_outval[17:0]	OUT	SIGNED18. Current control probe Y-output

vsmodval[16:0]	OUT	UNSIGNED17, Vs module
vsangval[31:0]	OUT	Vs angle
ismodval[16:0]	OUT	UNSIGNED17, Is module
isangval[31:0]	OUT	Is angle
smo_bemf_m[16:0]	OUT	UNSIGNED17, SMO Zs module
smo_bemf_p[31:0]	OUT	SMO Zs angle
mrt_angle[31:0]	OUT	Scalar mode IP angle
enc_angle[31:0]	OUT	Incremental encoder angle
hls_angle[31:0]	OUT	Hall sensors angle
rsv_angle[31:0]	OUT	Resolver angle
smo_angle[31:0]	OUT	SMO angle
rot_angle[31:0]	OUT	Rotor angle

Detailed Description

This module implements the system register for the set up and run time execution of the *motorfoc* module. The address space of the registers is divided in 4 zones. In the table below are reported the zones.

Address range	Zone type
0x00000 – 0x01FFF	Registers
0x02000 – 0x03FFF	Hall sensors angles DPR
0x04000 – 0x05FFF	-
0x06000 – 0x07FFF	-
0x08000 – 0x0FFFF	PWM waveform tables

In the following section is reported the map of the registers used by the module. All registers are 32 bits size. The register offset is “register index” * 4.

Registers description table

REGISTERS DESCRIPTION				
Address offset	Register index	Register name	Access	Description
0x00000	0	ip_ident	READ	Motor control IP identification
	1	tsclocks	READ	Measured cycle time (clocks)
	2	motor_control	R/W	Motor control
	3	motor_status	READ	Motor status / event
Read inverter input values				
	4	val_iphs_a	READ	Current phase-A
	5	val_iphs_b	READ	Current phase-B
	6	val_iphs_c	READ	Current phase-C
	7	val_ibus_x	READ	Current DC_link
	8	val_vphs_a	READ	Voltage phase-A
	9	val_vphs_b	READ	Voltage phase-B
	10	val_vphs_c	READ	Voltage phase-C
	11	val_vbus_x	READ	Voltage DC_link
	12	val_vphs_n	READ	Voltage neutral
Read and write inverter offset values				
	13	ofs_iphs_a	R/W	Current phase-A
	14	ofs_iphs_b	R/W	Current phase-B
	15	ofs_iphs_c	R/W	Current phase-C
	16	ofs_ibus_x	R/W	Current DC_link
	17	ofs_vphs_a	R/W	Voltage phase-A
	18	ofs_vphs_b	R/W	Voltage phase-B
	19	ofs_vphs_c	R/W	Voltage phase-C

REGISTERS DESCRIPTION				
Address offset	Register index	Register name	Access	Description
	20	ofs_vbus_x	R/W	Voltage DC_link
	21	ofs_vphs_n	R/W	Voltage neutral
	22	xbus_fk1	R/W	dc_link LPFT1 #1 const
	23	xbus_fk2	R/W	dc_link LPFT1 #2 const
	24	xphs_fk1	R/W	Phases LPFT1 #1 const
	25	xphs_fk2	R/W	Phases LPFT1 #2 const
	26	ibus_limit	R/W	Dc_link current limit
	27	iphs_limit	R/W	Phases current limit
	28	ismodmax	R/W	Is current limit
	29	ismodval	READ	Is real time current value
	30	isangval	READ	Is real time angle value
	31	vsmodval	READ	Vs real time modulo
	32	vsangval	READ	Vs real time angle
	33	rot_angdef	R/W	Rotor position reset angle
	34	rot_angle	READ	Rotor position angle
	Speed evaluation registers			
	35	spd_fktau1	R/W	Speed evaluation LPFT1 #1 const
	36	spd_fktau2	R/W	Speed evaluation LPFT1 #2 const
	37	spd_speed	READ	Speed evaluation current speed
	SMO Position evaluation registers			
	38	smo_vs_mult	R/W	Position Evaluation Vs multiplier
	39	smo_is_mult	R/W	Position Evaluation Is multiplier
	40	smo_zs_max	R/W	Position Eval BEMF max error
	41	smo_es1_kflt	R/W	Position Eval BEMF LPF1 #1
	42	smo_es2_kflo	R/W	Position Eval BEMF LPF1 #2 base
	43	smo_es2_kfmx	R/W	Position Eval BEMF LPF1 #2 mult
	44	smo_es2_kflt	READ	Position Eval BEMF LPF1 #2
	45	smo_angofs	R/W	Position Eval angle offset
	46	smo_bemf_p	READ	Position Eval BEMF Angle
	47	smo_bemf_m	READ	Position Eval BEMF Modulo
	48	smo_angle	READ	Position Eval Angle

REGISTERS DESCRIPTION				
Address offset	Register index	Register name	Access	Description
	49	pos_position	READ	Low resolution current position
Speed Loop Control				
	50	slp_spdset	R/W	Speed set point
	51	slp_kmpro	R/W	Proportional gain
	52	slp_kmint	R/W	Integrative gain
	53	slp_outlim	R/W	Current limit
	54	slp_kmultx	R/W	Current X multiplier
	55	slp_kmulty	R/W	Current Y multiplier
	56	paipol	R/W	Motor pair poles (1..n)
External rotor angle sensor				
	57	ext_angle	READ	External angle
Resolver angle sensor				
	58	rsv_m2rppk	R/W	Motor to Resolver Pair Poles Ratio
	59	rsv_angofs	R/W	Resolver angle offset
	60	rsv_angle	READ	Resolver angle
Hall sensor				
	61	hls_ctolim	R/W	Counter timeout limit
	62	hls_angle	READ	Hall sensor angle
Incremental encoder				
	63	enc_index	READ	Encoder index
	64	enc_phase	READ	Encoder phase
	65	enc_phcpt	READ	Encoder phase hold
	66	enc_cyprnd	R/W	Cycles per round
	67	enc_angphs	R/W	Encoder angle increments per phase
	68	enc_angle	READ	Encoder Electric rotor angle
Manual rotor angle				
	69	mrt_speed	R/W	Encoder simulator angle increments per netmot s-link packet (see detailed description)
	70	mrt_accmax	R/W	Acceleration limit
	71	mrt_fktau1	R/W	First LPF1 filter speed
	72	mrt_fktau2	R/W	Second LPF1 filter speed
	73	mrt_spdout	READ	Speed set
	74	mrt_angle	READ	Encoder simulator Electric rotor
Pi_control regulator for X_coordinate or D_frame and Y_coordinate or Q_frame				

REGISTERS DESCRIPTION				
Address offset	Register index	Register name	Access	Description
	75	pi_setvalx	R/W	Current loop X setpoint
	76	pi_setvaly	R/W	Current loop Y setpoint
	77	pi_kmpro	R/W	PI proportional gain multiplier
	78	pi_kmint	R/W	PI integrative error gain multiplier
Common modulators				
	79	mod2angskw	R/W	Second modoulator angle skew
PWM modulator				
	80	pwm_kmod	R/W	PWM gain multiplier
	81	pwm_presc	R/W	PWM prescaler
	82	pwm_mdmax	R/W	PWM modulation limit
	83	pwm_mdval	READ	PWM real time modulation value
	84	pwm_ctrl	R/W	PWM control register
RPFM modulator				
	85	rpfm3p_ctrl	R/W	PFM control register
	86	deadval	R/W	Gate unit dead time value
	87	gwswcnt	R	Gate unit switches counter
Hall Sensors angles LUT				
0x02000	0..15	hls_dprangle[0..15]	R/W	Angles LUT for hall sensor IP
PWM table addresses				
0x08000	0..255	pwm_waveform_0[0...255]	R/W	PWM waveform table 0
	256..511	pwm_waveform_1[0...255]	R/W	PWM waveform table 1
	512..767	pwm_waveform_2[0...255]	R/W	PWM waveform table 2
	768..1023	pwm_waveform_3[0...255]	R/W	PWM waveform table 3

Motor_ip_ident - Motor IP identification register

This register reports the IP identification register.
The current value is for test purpose only.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
24..31	lp_id_code	READ	1	Code
16..23	lp_id_majv	READ	1	Major version
8..15	lp_id_minv	READ	2	Minor version
0..7	lp_id_hscrt	READ	97	H/W S/W compatibility

TSclocks - FOC clock cycles

This register reports the number of system clocks between two consecutive FOC activation

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
12..31		READ	0	Unused/reserved
11..0	tsclocks	READ	-	System clocks on FOC cycle

Motor_control - Motor control register

This register controls the FOC IP.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
28..31		READ	0	Unused/reserved
27	smo_usevsact	R/W	0	SMO Vs selector: 0=target, 1=measured
26	zerovphsx	R/W	0	Zero motor voltage phases (0->1 only)
25	zerovbusx	R/W	0	Zero dc_link voltage (0->1 only)
24	reseterr	R/W	0	Reset latched error
23	zerocurr	R/W	0	Zero current offset command (0->1 only)
22	slp_mrt2spd	R/W	0	Pos&Speed: MRT to Speed loop link
21	slp_spd2trq	R/W	0	Speed loop feeds the current loop
20	enc_xmcha	R/W	0	Encoder CH-A match for index event
19	enc_xmchb	R/W	0	Encoder CH-B match for index event
18	enc_xmchi	R/W	0	Encoder CH-I match for index event
17	enc_inten	R/W	0	Encoder interpolator enable
16	enc_rstang	R/W	0	Encoder electric rotor angle evaluation reset control 1=reset-lock, 0=running
15		READ	0	Unused/reserved
14	mrt_rstang	R/W	0	Encoder emulator electric rotor angle evaluation reset control 1=reset-lock, 0=running

13	smo_rstang	R/W	0	Position Eval electric rotor angle reset control 1=reset-lock, 0=running
12	fbk_angdef	R/W	0	Default angle selector 0=default register 1=rot_angle feedback
11	pi_deafmd	R/W	0	PI current feedback control 1=ignore feedback, 0=use feedback
10	is3phases	R/W	0	1=3-phase motor, 0=stepper motor
9..8	modlevels	R/W	0	0=2-levels, 1=3-levels
7..4	rot_select	R/W	0	Rotor selector angle: 0>manual : "rot_angdef" register, 1=MRT : scalar mode, 2=ENC : incremental encoder, 3=SMO : sliding mode observer, 4=HLS : hall sensors, 5=RSV : resolver, 6=EXT : external sensor
3..2	modtype	R/W	0	Modulator selector request 0=PWM 1=RPFM
1		READ	0	Unused/reserved
0	coilenab	R/W	0	Coil enable 1=IP control, 0=drive LOW

Motor_status - Motor status register

This register report FOC status and let reset of latched events.
The read access freeze some status registers for atomic read.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unused/reserved
16	hwkill	READ	0	Kill input from Gate unit
15	hwfail	READ	0	H/W failure from Gate unit
14	ovi_iphs_a	READ	0	Overcurrent motor Phase-A
13	ovi_iphs_b	READ	0	Overcurrent motor Phase-B
12	ovi_iphs_c	READ	0	Overcurrent motor Phase-C
11	ovi_ibus_x	READ	0	Overcurrent dc_link
10	syserr	READ	0	Global system error
9	spare_9	READ	0	-
8	spare_8	READ	0	-
7	spare_7	READ	0	-
6..5	rpfmzmd	READ	0	RPFM modulation zone 0=IDLE (not operational) 1=Sinusoidal/Extended sinusoidal(linear zone)

				2=Hexagon zone (partial saturation) 3=Saturation zone (square wave or six step)
4	modtype0	READ	0	Modulator type in use 0=PWM, 1=RPFM
3	spd_fwdir	READ	0	speed evaluation moving direction 1=FWD, 0=REV
2	spd_moving	READ	0	speed evaluation moving status 1=moving, 0=still
1	pwm_mdovf	READ	0	PWM modulation overflow
0	lsmodover	READ	0	Is current overflow. The 1=overflow will stop the motor to a safe condition. The event reset requires switch off the motor writing "0" in coil enable control register bit

Inverter values from A/D acquisition.

This register returns the voltage and current of motor phases and dc-link. The values are normalized as SIGNED18

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
18..31		READ	0	Unused/reserved
0..17	val_iphs_a val_iphs_b val_iphs_c val_ibus_x val_vphs_a val_vphs_b val_vphs_c val_vbus_x val_vphs_n	READ	0	Motor Phase-A current Motor Phase-B current Motor Phase-C current Dc_link current Motor Phase-A voltage Motor Phase-B voltage Motor Phase-C voltage Dc_link voltage Motor neutral voltage

The value is SIGNED18. For external representation in "Amperes" and "Volts", multiply by proper gain floating point constant.

BIT NUMBER/INDEX	INVERTER ANALOG CHANNEL
0	IPHS_A
1	IPHS_B
2	IPHS_C
3	IBUS_X
4	VPHS_A
5	VPHS_B
6	VPHS_C
7	VBUS_X
8	VPHS_N

The configuration constant C_INV_IN_MAP is used to define the number of active channel. The configuration constant C_INV_IN_NOT is used to force two complement values (for negative inputs). Both constant are integer bit mask where each bit refer a specific analog channel. The default value 131 (decimal) in C_INV_IN_MAP correspond to binary value '01000011b'. This means the IPHS_A, IPHS_B and VBUS_X are implemented.

Inverter offset value.

This register let set/get the offset values for zero calibration for each analog channel. The values are normalized as SIGNED18

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
18..31		READ	0	Unused/reserved
0..17	ofs_iphs_a ofs_iphs_b ofs_iphs_c ofs_ibus_x ofs_vphs_a ofs_vphs_b ofs_vphs_c ofs_vbus_x ofs_vphs_n	R/W	0	Motor Phase-A current Motor Phase-B current Motor Phase-C current Dc_link current Motor Phase-A voltage Motor Phase-B voltage Motor Phase-C voltage Dc_link voltage Motor neutral voltage

These register let zero calibration of analog acquisition system. Two method of zero calibration are allowed if enabled in C_INV_OFSV_MODE.

BIT	NAME	DEFAULT	DESCRIPTION
1	ZERO_SW	0	Individual offset register can be set
0	ZERO_AUTO	1	Automatic zero function on command

xbus_fk1, xbus_fk2 – DC_LINK LPF1 parameter register

These registers are used to setup the cutting frequency of LPF1 used to filter the dc_link both voltage and current.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unused/reserved
0..16	xbus_fk1/xbus_fk2	R/W	0	LPF1 multiplier constant in range 0..2 ¹⁷ -1

A second order filter is implemented using two LPF1 first order filters in cascade configuration. The `xbus_fk1` is used to configure the first filter, and the `xbus_fk2` is used to configure the second filter.

The filter IP is enabled if `C_INV_FILTER = 1`.

xphs_fk1, xphs_fk2 – Motor phases LPF1 parameter register

These registers are used to setup the cutting frequency of LPF1 used to filter the motor phases both voltage and current.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unused/reserved
0..16	<code>xphs_fk1/xphs_fk2</code>	R/W	0	LPF1 multiplier constant in range $0..2^{17}-1$

A second order filter is implemented using two LPF1 first order filters in cascade configuration. The `xphs_fk1` is used to configure the first filter, and the `xphs_fk2` is used to configure the second filter.

The filter IP is enabled if `C_INV_FILTER = 1`.

ibus_limit – current limit for dc_link

The register is used to set the `dc_link` current limit to protect the inverter and `dc_link` source from overcurrent.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	<code>ibus_limit</code>	R/W	0	<code>dc_link</code> current limit

iphs_limit – current limit for motor phases

The register is used to set the motor phases current limit to protect the inverter, and the motor from overcurrent.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	<code>iphs_limit</code>	R/W	0	Motor phases current limit

Ismodmax – Is current limit

The register is used to set the Is current limit to protect the motor against overcurrent. The FOC IP monitor the Is current and compare the value with the defined limit. In case of overflow the ismodover bit is set into motor status register: the motor will stop immediately and coil driver will be set to neutral position.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	ismodmax	R/W	0	Is current limit

Ismodval – Is current value

The read only register report the real time Is current modulo.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	ismodval	READ	0	Is current modulo

Isangval – Is current angle

The read only register report the real time Is current angle. The value resolution is $2^{32}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	isangval	READ	0	Is current angle

Vsmodval – Vs voltage value

This read only UNSIGNED17 register reports the real time Vs voltage modulo. The bit resolution depend on h/w implementation for proper interface with final motulator

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	vsmodval	READ	0	Vs voltage modulo

Vsangval – Vs voltage angle

This read only register reports the real time Vs voltage angle. The value resolution is $2^{32}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	vsangval	READ	0	Vs voltage angle

rot_angdef – rotor initial angle

This register is used to set the initial angle value for all position IP cores. The value is defined as electric rotor angle. The value is loaded at h/w and manual reset of IP. The register is UNSIGNED32 value with $2^{32}=360$ degrees. With number of pair poles = 1 the angle correspond to mechanical rotor angle.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	rot_angdef	R/W	0	Initial angle for position IP cores

rot_angle – rotor angle

This read only register contains the real time angle generated by IP. The angle resolution is $2^{32}=360$ degrees. The value is loaded from selected IP cores according to rot_selector defined in motor control register. In case of IP core reset, rot_angle assumes the value according to rot_selector and fbk_angdef values.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	rot_angle	READ	0	Angle value

Spd_fktau1, spd_fktau2 – Speed evaluation LPF1 parameter register

These registers are used to setup the cutting frequency of LPF1 used in speed evaluation IP core.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unused/reserved
0..16	Spd_fktau1/spd_fktau2	R/W	0	LPF1 multiplier constant in range $0..2^{17-1}$

A second order filter is implemented using two LPF1 first order filters in cascade configuration. The spd_fktau1 is used to configure the first filter, and the spd_fktau2 is used to configure the second filter.

The LPF1 formula is the following: $Y = Y + (X - Y) * K$

Where:

Y = internal accumulator and result;

X = new current sample;

K = error weight in range 0...1.

The spd_fktau1/2 register is an UNSIGNED17 value in range 0...131071 for a corresponding:
 $K = [0/2^{17} \dots (2^{17}-1)/2^{17}]$.

The filter function is executed for every IP activation. Refer to LPF1 IP for details.

Spd_speed – Speed evaluation current speed register

The speed is evaluated by integration of “rot_angle” signal that correspond of electric speed of rotor.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	spd_speed	READ	0	SIGNED32 speed value

The speed is defined as angle/time where:

Angle is the register content in range $-2^{31}..2^{31}-1$ that correspond to: $A = \text{value} / 2^{32} * 2 \pi$

The time is defined by IP core activation time.

Example: the value 1374390 with 3.2 μSec of IP core activation time correspond to about 100 Hz

NOTE: The speed is defined as electric speed.

smo_vs_mult – position evaluation Vs multiplier

The value is an UNSIGNED32 multiplier used by the position evaluation IP core. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	smo_vs_mult	R/W	0	Vs multiplier

smo_is_mult – position evaluation Is multiplier

The value is an UNSIGNED32 multiplier used by the position evaluation IP core. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	smo_is_mult	R/W	0	Is multiplier

smo_zs_max – position evaluation maximum error

The value is an UNSIGNED17 that represents the absolute maximum error in the BEMF evaluation. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_zs_max	R/W	0	Absolute max BEMF error

smo_es1_kflt – position evaluation BEMF LPF1 #1

The value is an UNSIGNED17 that sets up the first LPF1 used to evaluate the BEMF. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_es1_kflt	R/W	0	LFP1 #1 filter coefficient for BEMF evaluation

smo_es2_kflo – position evaluation BEMF LPF1 #2

The value is an UNSIGNED17 that sets up the second LPF1 used to evaluate the BEMF. The value is used to define the minimum Fcut for speed=0.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_es2_kflo	R/W	0	LFP1 #2 filter coefficient for BEMF evaluation

smo_es2_kfmx – position evaluation BEMF LPF1 #2

The value is an UNSIGNED17 that sets up the second LPF1 used to evaluate the BEMF. The value is used to extend the Fcut according speed. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_es2_kfmx	R/W	0	LFP1 #2 filter coefficient for BEMF evaluation

smo_es2_kflt – position evaluation BEMF LPF1 #2

The value is an UNSIGNED17 that sets up the second LPF1 used to evaluate the BEMF. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_es2_kflt	READ	0	LFP1 #2 filter coefficient for BEMF evaluation

smo_angofs – position evaluation angle offset

The value is an SIGNED16 angle value in range $[-\pi.. \pi]$ to compensate the bemf output angle on SMO.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
16..31		READ	0	Unassigned/reserved
0..15	smo_angofs	R/W	0	Angle offset

smo_bemf_p – position evaluation BEMF angle

Read only UNSIGNED32 register. It represents the BEMF vector angle. The value 2^{32} corresponds to 360 degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	smo_bemf_p	READ	0	BEMF vector phase

smo_bemf_m – position evaluation BEMF modulo

Read only UNSIGNED17 register. It represents the BEMF vector modulo. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	smo_bemf_m	READ	0	BEMF vector modulo

smo_angle– position evaluation rotor electric angle

Read only UNSIGNED32 register. It represents the rotor electric angle (flux vector). The value 2^{32} corresponds to 360 degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	smo_angle	READ	0	Rotor electric angle (2^{32})

Pos_position– low resolution position rotor electric angle

Read only SIGNED32 register. The range is $-2^{31}..2^{31}-1$. The value 2^{16} corresponds to 360 degrees. The range rounds is $-2^{15}..2^{15}-1$. The value represents the current rotor electric angle according the selected rotor control come.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	pos_position	READ	0	Rotor electric angle (2^{16})

slp_spdset– speed setpoint for speed loop control

Read/Write SIGNED32 register. Refer to ***spd_speed*** register for unit definition.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	slp_spdset	R/W	0	Speed setpoint

The speed setpoint is used in speed loop when ***spd2trq***=1 to feed the current loop. The speed loop is also used to feed the position loop when ***spd4pos***=1.

slp_kmpro- speed proportional error gain for speed loop control

Read/Write IEEE-754 32-bits FLOAT register. The proportional gain is $slp_kmpro / 2^{P_SLP_PRO_DLN2}$.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	slp_kmpro	R/W	0	Proportional error gain

slp_kmint - speed integrative error gain for speed loop control

Read/Write IEEE-754 32-bits FLOAT register. The integrative gain is $slp_kmint / 2^{C_SLP_INT_DLN2}$.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	slp_kmint	R/W	0	integrative error gain

slp_outlim - speed output current limit

Read/Write UNSIGNED17 register. The values is the current limit for speed control loop.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	slp_outlim	R/W	0	Current limit

slp_kmultx, slp_kmulty- speed output current multiplier

Read/Write SIGNED18 registers. The values is a $K / 2^{16}$ multiplier for X/Y current output setpoint.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
18..31		READ	0	Unassigned/reserved
0..17	slp_kmultx slp_kmulty	R/W	0	Current X/Y control.

The effective gain are usually evaluated by:

$$slp_kmultx = \cos(\text{angle}) * 2^{16}$$

$$slp_kmulty = \sin(\text{angle}) * 2^{16}$$

The angle value for maximum torque is $\pi/2$.

Paipol – motor pair poles

This register setup the number of motor pair poles.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
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8..31		READ	0	Unused/reserved
0..7	paipol	R/W	0	Motor pair poles in range 1..255

The number of pair poles (“pair-poles” = “poles / 2”) is used on several sub functional IP. Set the proper value in range “1..n” according motor characteristics.

IMPORTANT: do not set value “0” (zero).

ext_angle – External sensors angle

This read only register contains the real time angle generated by external sensors IP. The angle resolution is $2^{32}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	ext_angle	READ	0	Angle value

rsv_m2rppk – Motor to Resolver Pair Poles Ratio

This register defines the ratio between motor pair poles and resolver pair poles.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
8..21		READ	0	Unassigned/reserved
0..7	rsv_m2rppk	R/W	1	Pair Poles Ratio = Motor PP / Resolver PP

Example: if motor pair poles is 6, and resolver pair poles is 2, the register shall be set to 3.

rsv_angofs – Resolver sensors angle offset

This register SIGNED16 set the angle offset to correct alignment between resolver sensor and motor flux. The angle resolution is $2^{16}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
16..31		READ	0	Unassigned/reserved
0..15	rsv_angofs	R/W	0	Angle value

rsv_angle – Resolver sensors angle

This read only register contains the real time angle generated by resolver sensors IP. The angle resolution is $2^{32}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	rsv_angle	READ	0	Angle value

hls_ctolim – Hall sensors coasting mode counter timeout limit

This r/w register contains the clock timeout for coasting mode used to control the angle interpolator. The value is system clock units.

Example: with system clock @ 100 mHz, the maximum value $2^{20}-1$ is about 10.5 msec.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
20..31		READ	0	Unassigned/reserved
0..19	hls_ctolim	R/W	0	Timeout value

hls_angle – Hall sensors angle

This read only register contains the real time angle generated by hall sensors IP. The angle resolution is $2^{32}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	hls_angle	READ	0	Angle value

enc_index – Encoder index register

It counts the index rising edges pulses or motor revolutions. This register is unipolar (unsigned) and is incremented regardless of rotation direction (forward or reverse).

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	enc_index	READ	0	Rounds counter

enc_phase – Encoder phase register

It counts the sensor phases. This register is bipolar (signed). The counter is incremented in forward direction and decremented in reverse direction. The counter counts four phases for each encoder pulse. If the register size is less than 32 bits then the most significant bits are at fixed value of “0” (no signed extend function is applied).

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	enc_phase	READ	0	Phases counter

Enc_phcpt - Encoder phase hold

The register hold Enc_phase on rising edge of encode index. The first sampled value corresponds to index position at power on, all others values are: initial_offset + revolutions * phases_per_revolutions.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	enc_phcpt	READ	0	Phases counter.

enc_cyprnd - Encoder cycles per round

This UNSIGNED12 register is used to set the pulses (or cycles) per round for the given encoder. An encoder pulse correspond to 4 phases. The value limit is 4095 pulses or 16380 phases.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
12..31		READ	0	Unassigned/reserved
0..11	enc_cpyrnd	R/W	0	Angle increment per phase.

enc_angphs - Encoder angle increment

This register is used to set the angle increment for each phase transition. For a given encoder of 256 pulses per round we have $256 \times 4 = 1024$ phases per mechanical round. If the motor have 2 pair poles (2=electric rounds for each mechanical round), the electric rotor phases per rounds are $1024 / 2 = 512$. The angle resolution is $2^{32} = 360$ degrees, so the register shall be set to $2^{32} / 512 = 8388608$.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	enc_angphs	R/W	0	Angle increment per phase.

Enc_angle - Encoder angle

This read only register contains the real time angle generated by encoder IP. The angle resolution is $2^{32} = 360$ degrees. The H/W reset or IP user reset can be used to force load of enc_angdef value.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	enc_angle	READ	Enc_angdef	Angle value

Mrt_speed - scalar mode rotor speed setpoint

This register is used to set the angle increment for each internal time base event.

Example:

IP cycle time = 3.2 μ S,

Motor Pair Poles = 2,

Desired speed = 1000 RPM = 16.667 RPS (round per seconds) Rotor Electric speed = 16.667 RPS * 2 pair poles = 33.333 Hz (flux speed is electric rotor speed)
Enc_mrtspeed = 33.333 Hz / 3.2⁻⁶ = 10,416,667

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	mrt_speed	R/W	0	Speed set point

The **mrt_speed** is used directly when C_MANROT = 1,
If C_MANROT = 2 the maximum acceleration is applicable and a double LPF1 filter is used to smooth the effective speed.

Mrt_accmax – scalar mode rotor acceleration limit

This register is used to control the speed ramp from current speed to target speed.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	mrt_accmax	R/W	0	Acceleration limit

The value is application with C_MANROT = 2.

Mrt_fktau1/mrt_fktau2 – scalar mode rotor double LPF1filters

The value is an UNSIGNED17 that sets up the first LPF1 used to smooth the speed setpoint in scalar mode rotor control. Refer to the specific IP document for a detailed description.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	mrt_fktau1 mrt_fktau2	R/W	0	LFP1 filter coefficient for speed value

Mrt_spdout – scalar mode rotor speed value

This read only register report the speed value after double LPF filter.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	mrt_spdout	READ	0	Speed value

Mrt_angle – scalar mode rotor angle

This read only register contains the real time angle generated by encoder emulator IP. The angle resolution is $2^{32}=360$ degrees. The H/W reset or IP user reset can be used to force load of **enc_angle** value.

The encoder emulator IP input default value is internally connected to encoder IP angle output for a cascade operation. The encoder emulator is in reset=inhibit state, the encoder angle output pass through the encoder emulator.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	mrt_angle	READ	Enc_angle	Angle value

Pi_setvalx, pi_setvaly – PI setpoint value

These registers are a SIGNED18 bit values used to setup the desired X/Y currents. The value is compared with current feedback to evaluate the Vs vector. The bit resolution depends on h/w implementation.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
18..31		READ	0	Unassigned/reserved
0..17	pi_setvalx pi_setvaly	R/W	0	Current setpoint

Pi_kmpro – PI proportional error multiplier

The register is a proportional error multiplier for error gain.

The effective value is $pi_kmpro / 2^{C_PI_ERPRO_DIVLN2}$.

The value is used for both **kmpro_x** and **kmpro_y** internal signals.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	pi_kmpro	R/W	0	Proportional error multiplier

Pi_kmint – PI integrativ error multiplier

The register is a integrative error multiplier for error gain.

The effective value is $pi_kmint / 2^{C_PI_ERINT_DIVLN2}$.

The value is used for both **kmint_x** and **kmint_y** internal signals.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	pi_kmint	R/W	0	Integrator error multiplier

Mod2angskw – second modulator angle skew

In double independent 3-phases windings of BLDC/PMSM motor, this register SIGNED16 shall be programmed with angle offset of 2nd winding.

The angle resolution is $2^{16}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
16..31		READ	0	Unassigned/reserved
0..15	mod2angskew	R/W	0	Angle value

Pwm_kmod – PWM modulation multiplier

The register is a multiplier applied to Vs voltage modulator for scale correction (PWM frequency and DC_link compensation).

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	pwm_kmod	R/W	0	Pwm argument multiplier

Pwm_presc – PWM prescaler

Two PWM prescaler UNSIGNED17 bit register is used to set the PWM frequency. The PWM wave generator runs at main clock frequency.

The value width is 17 bits for a range in $0...2^{17}-1$.

The PWM frequency is obtained by this formula: $pwm_presc = sysclock / pwm_freq / 2 - 1$

Example for system clock of 50 MHz and desired pwm_freq of 20 KHz;

$Pwm_presc = 50 \text{ MHz} / 20 \text{ KHz} / 2 - 1 = 1249$.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	pwm_presc	R/W	0	PWM prescaler value: range is $0...2^{17}-1$

Pwm_mdmax – PWM modulation limit

This register is used to limit the modulation duty cycle to desired value. The bit resolution is the same of pwm_presc.

The PWM modulator compares the PWM modulation value with the pwm_mdmax limit. In case of overflow the pwm_mdovf bit of motor status register is set.

It is highly recommended to set this register at a proper value in order to protect the gate power stage against too long high side driver time ON.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	pwm_mdmax	R/W	0	PWM modulation limit value: range is $0.. 2^{17}-1$

Pwm_mdval – PWM modulation value

This read only register report the real time modulation value. The value is in range 0...pwm_mdmax with pwm_presc = 100%.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
17..31		READ	0	Unassigned/reserved
0..16	pwm_mdval	READ	0	PWM modulation limit value: range is 0.. .. 2 ¹⁷ -1

Pwm_ctrl – PWM control register

This register selects various option of PWM modulaor.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
3..31		READ	0	Unassigned/reserved
2	cmmofs	R/W	0	3-Phase common mode offset
0..1	table	R/W	0	PWM modulation table selector

Rpfm3p_ctrl – PFM control register

This register controls the PFM parameters setup.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
14..31		READ	0	Unassigned/reserved
13	rpfm3p_v7h	R/W	0	Null vector 7 hold mode: 0=vector 7 fall to vector 0 1=vector 7 hold for reduced switches
12	rpfm3p_v07n	R/W	0	Null vector 0/7 transition mode: 0=vector 0 1=vector 0 or 7 is selected for reduced switches
8..11	rpfm3p_mdpr	R/W	0	RPFM modulator prescaler 0..15
0..7	rpfm3p_mdkd	R/W	0	RPMF modulator clock divider 0..255

Vector 0/7 nice (v07n)	Vector 7 hold (v7h)	Vector 0/7 modes
0	x	Vector 7 disable
1	0	Vector 7 only one shot
1	1	Symmetric mode

The modulator pulse width is defined by system clock divider.

$$\text{clock_divider} = (\text{rpfm3p_mdkd} + 1) * (\text{rpfm3p_mdpr} + 1)$$

Example:

IP core activation time = 3.2 μ S,
 System clock = 62.5 MHz,
 Desired modulation pulse width = 6.4 μ S,
 Rpfm3p_mdcd = 24
 rprm3p_mdpr = 15

Refer to RPFM specific IP datasheet for details and limitations.

deadval – Gate unit dead time value

This register can be used to set value for gate unit dead time.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
8..31		READ	0	Unassigned/reserved
0..7	deadval	R/W	255	Value for gate unit dead time

The value is not used in motor control IP. The signal is delivered to gate unit IP as-is.

gswswcnt – Gate unit switches counter

This register can be used to report the gate unit switches

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
0..31	gswswcnt	0	-	Value from gate unit

The value is not used in motor control IP. The signal is reported from gate unit.

hls_dprangle[0...15] – hall sensor DPR angles

This set of 16 registers is used by the hall sensor IP to evaluate the motor electric angle. Look to specific IP description.

The angle resolution is $2^{16}=360$ degrees.

BIT	NAME	ACCESS	RESET VALUE	DESCRIPTION
16..31		READ	0	Unassigned/reserved
0..15	hls_dprangle[0...15]	R/W	0	16 bits SIGNED value

pwm_waveform[0...1023] – PWM waveform DPR

A set of four PWM waveform tables are defined using a single Xilinx BRAM 1024x18 primitive.

The DPR can be accessed in R/W modes from host side and READ only from PWM IP side.

The four tables are addressed by vector index range:

Table 0: 0...255

Table 1: 256...511

Table 2: 512...767

Table 2: 768...1023

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from ZYNQ 7-family of FPGAs. The following tables lists the devices used for characterization using default IP parameters.

Device Utilization Summary (estimated values)	
Logic Utilization	ZYNQ
Number of LUT	7355
Number of FF	7645
Number of BRAM	4
Number of LUTRAM	32
Number of DSP	24

Execution time

Start event	End of execution	clock cycles¹	Time @ 50 MHz	Time @ 100 MHz
Curr_sync	Pwm(2-phases)	188	3.76 μS	1.88 μS
Curr_sync	Pwm(3-phases)	201	4.04 μS	2.01 μS
Curr_sync	RPFM(3-phases)	172	3.44 μS	1.72 μS

¹ Unless otherwise noted.

Reference Documents

n/a

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
16/09/2011	1.0	QDeSys first release.
19/11/2011	1.1	Added some registers. Modified Devices Utilization table. Removed pwm_dmod register.
23/12/2011	1.2	Correct execution time table. Update for new PI_control IP
23/03/2012	1.3	Updated registers
12/05/2012	1.4	Added Kintex 7 and Zynq support
11/07/2013	1.5	Position and speed loop control. BEMF feed forward compensation. Register map review.
13/05/2014	1.6	Hall sensor IP, double 3-phase modulator, enhanced feature for MRT IP.
14/02/2015	1.7	RPFM 3-levels modulator, Resolver sensor IP, extra trigger in current acquisition, direct access to dc_link and currents.
19/05/2016	1.8	Inclusion of analog preprocessing IP for offset, filtering and zero offset. Extend interface to motor board specific IP for diagnostic and probes.
6-Jan-17	1.9	Update speed loop, update current loop, remove bemf compensation
March 21, 2017	1.10	Remove acquisition feature. Optimized PI-control
August 6, 2017	1.11	Added PI current control probes, resolver ip update
20-Dec-17	1.12	Motor status register modification and PWM control register added.
June 1, 2018	1.13	Update interface for MRT acceleration scaling
June 27, 2019	1.14	Update control register

September 6, 2019	1.15	Resolver pair poles ratio added. Correct some register definitions
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