FUNCTION

Proportional Integral (PI) control.

VHDL File

pi_control.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A/A1/E1

Sub modules used

dsp4mot.vhd

Execution time

5 clocks to finish
6..14 clocks to ready

Introduction

This IP realizes a standard PI (Proportional Integral) regulator with anti-windup control. The PI uses the rectangular integration and the generic formula is:

$$u_n = K_p e_n + K_i \frac{T}{T_i} \sum_{k=0}^{n} e_n$$

Equation 1: generic PI regulator

Where:

u_n is the output value at the time n*T
e_n is the error at the time n*T
K_p is the proportional gain
K_i is the integrative gain
T_i is the time constant of the integral
T is the sampling period

Detailed Description

This module implements a PI (Proportional Integral) regulator and the implemented formula is

$$u_n = K_{mpro} e_n 2^{-c\_erpro\_dln2} + K_{mint} 2^{-c\_erint\_dln2} \sum_{k=0}^{n} e_n$$

Equation 2: PI formula of the IP core

The calculation begins when the ***start*** signal is driven high for 1 clock cycle; the process terminates when the module sets the ***finish*** signal high for 1 clock cycle.

The set-point of the PI is the ***setval[17:0]*** SIGNED18 argument and the feedback value is the ***fbkval[17:0]*** SIGNED18 argument. The error is calculated as ***setval[17:0]***- f***bkval[17:0]***.

The integrative accumulator is post increment of : e_n
The anti-windup is implemented by post icremenent of : $-e_n 2^{-c\_wuint\_dln2}$

The ***kmpro[16:0]*** UNSIGEND17 argument is the multiplier of the proportional part of the PI module; referring to Equation 1 and Equation 2

kmpro[16:0] / $2^{c\_erpro\_dln2} = K_p$.

The ***kmint[16:0]*** UNSIGNED17argument is the multiplier of the integrator part of the regulator; referring to Equation 1 and to Equation 2

$$\frac{\boldsymbol{kmint}[\mathbf{16}:\mathbf{0}]}{\mathbf{2}^{\boldsymbol{c\_erint\_dln2}}} = K_p \left(\frac{T}{T_i}\right)$$

The ***outval[17:0]*** SIGNED18 output is the result of the calculation. The data is valid when ***finish*** is set high for 1 clock cycle and stay valid until the next ***finish*** signal or ***reset*** is set high. ***Outval[17:0]*** is saturated to ±131071.

The ***deafmd*** input is a flag used to ignore the ***fbkval[17:0]*** parameter, so that the error value is equal to the set point (***setval[17:0]***) and the PI block works in open loop. This option will exclude the integral part of equation.

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	zynq	Xilinx FPGA Family name
C_ERPRO_DLN2	integer	8..28	12	Base 2 logarithm of proportional error divisor
C_ERINT_DLN2	integer	8..28	18	Base 2 logarithm of integrative error divisor

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start calculation. Active high. The pulse width must be of 1 clock cycle.
offint	IN	Disable integrator.
deafmd	IN	Ignore fbkval[17:0]. Active high. If this signal is asserted the PI regulator works in open loop. The integrator is disabled.
setval[17:0]	IN	Set point (SIGNED18) of the regulator.
fbkval[17:0]	IN	Feedback value (SIGNED18).
kmpro[16:0]	IN	Proportional gain of the regulator (UNSIGNED17).
kmint[16:0]	IN	Integral gain of the regulator (UNSIGNED17).
outval[17:0]	OUT	Result of the regulator (SIGNED18).
finish	OUT	Output available. Active high. The pulse width is of 1 clock cycle.
ready	OUT	Ready for next cycle Active high. The pulse width is of 1 clock cycle.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	204
Number of Slice LUTs	329
Number of fully used LUT-FF pairs	201
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	5
ready	start	6..14

[1] Unless otherwise noted.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

QDESYS cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Ordering Information

For information on pricing and availability of QDESYS modules and software, please contact info@qdesys.com

Revision History

Date	Version	Description
08/07/2011	1.0	Initial QDeSys release
22/12/2011	1.1	Changed math & parameters for fast and fixed execution time
12/05/2012	1.2	Added Kintex 7 and Zynq support
5-Jan-17	1.3	Extend integral accumulator and remove bandwidth
March 21, 2017	1.4	Antiwindup modification for clipping.

Disclaimer

In disclosing the information contained in this document QDeSys assumes no obligation to correct any errors herein contained, or to advise you of any corrections or updates. QDeSys expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the information.

THE DOCUMENTATION IS DISCLOSED TO YOU "AS-IS" WITH NO WARRANTY OF ANY KIND. QDESYS MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE DOCUMENTATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS. IN NO EVENT WILL QDESYS BE LIABLE FOR ANY CONSEQUENTIAL, INDIRECT, EXEMPLARY, SPECIAL, OR INCIDENTAL DAMAGES, INCLUDING ANY LOSS OF DATA OR LOST PROFITS, ARISING FROM YOUR USE OF THE DOCUMENTATION