FUNCTION

Arctangent2 function

VHDL File

atan2.vhd

Applicable Devices

Spartan 3A DSP, Spartan 6, Kintex 7, Zynq

Xilinx primitive used

DSP48A
RAMB16_S18_S18

Sub modules used

dsp48a4m.vhd
idivision.vhd
bram1k18.vhd

Execution time

43 clocks

Introduction

The IP calculates the function atan2(y,x), which is defined as the angle between the positive x-axis and the (x,y) point on a Cartesian plane.

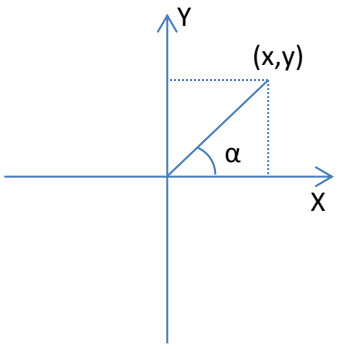

Figure 1: α=atan2(y,x)

Detailed Description

This module executes the arctangent function on input arguments. The equivalent function is:

$$resP = \tan^{-1}\left(\frac{argY}{argX}\right)$$

The arguments ***argX[17:0]***, ***argY[17:0]*** are defined as SIGNED18 variable and the range is -131072 to 131071.
The output ***resP[19:0]*** is defined as UNSIGNED20 and represent the normalized angle.
The effective angle in degrees is:

$$\alpha = \frac{resP}{2^{20}} \cdot 360$$

where α is the angle expressed in degree.
The process begins with the ***start*** command and the end of the process is notified by the ***finish*** flag.

In Table 1 there are the values that gets ***resP[19:0]*** for special values of ***argX[17:0]*** and ***argY[17:0].***

argX, argY	resP	mathematical theoretical value
0,0	131068	undefined
0,argY with argY>0	262144	90°
0,argY with argY<0	786432	270°

*Table 1: values of **resP[19:0]** for special cases of **argX[17:0]** and **argY[17:0]***

PARAMETERS

Parameter	Type	Values	Default	Description
C_FAMILY	string	spartan3adsp spartan6 kintex7	spartan3adsp	Xilinx FPGA Family name

SIGNALS

Signal	I/O	Description
clock	IN	Clock (rising edge).
reset	IN	Reset. Active high.
start	IN	Start the calculation. The pulse width must be of 1 clock cycle.
argX[17:0]	IN	Input X argument (SIGNED18). The range is -131072 to 131071.
argY[17:0]	IN	Input Y argument (SIGNED18). The range is -131072 to 131071.
resP[19:0]	OUT	Result (UNSIGNED20). The angle is: $\alpha = \frac{resP}{2^{20}} \cdot 360$, where α is the atan2(argX, argY) in degrees.
finish	OUT	End of the calculation. Active high. The pulse width is of 1 clock cycle.

TIMING PERFORMANCE AND RESOURCE USAGE

This section provides data on the timing performance and resource utilization of the core. Performance has been obtained on one representative device from the Spartan-3 Generation and Spartan 6 families of FPGAs. The following tables lists the devices used for characterization.

Device Utilization

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan3A DSP**
Number of Slices	203
Number of Slice Flip Flops	197
Number of 4 input LUTs	364
Number of BRAMs	1
Number of DSP48s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Spartan 6**
Number of Slice Registers	195
Number of Slice LUTs	330
Number of fully used LUT-FF pairs	183
Number of Block RAM/FIFO	1
Number of DSP48A1s	1

Device Utilization Summary (estimated values)	
Logic Utilization	**Kintex 7**
Number of Slice Registers	188
Number of Slice LUTs	338
Number of fully used LUT-FF pairs	177
Number of Block RAM/FIFO	1
Number of DSP48E1s	1

Execution time

output	input	clock cycles[1]
finish	start	43

[1] Unless otherwise noted.

Timing[2]

In the figure below there are the timings relative to a whole start/finish cycle of calculation.

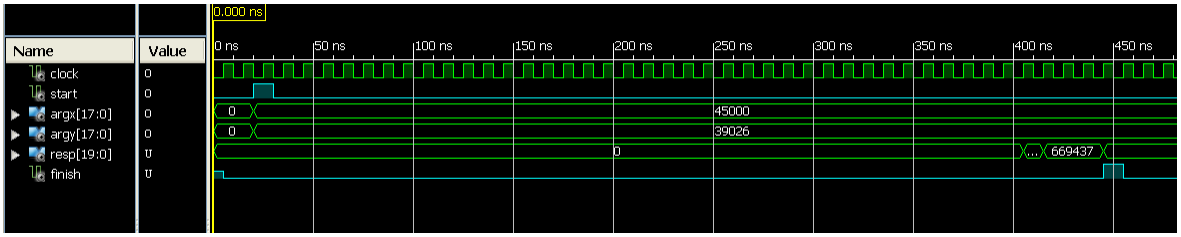

Figure 2: timings of a whole start/finish cycle

The process begins on the rising edge of the clock when the ***start*** signal is high; all the input signals must be stable when ***start*** is set high and they must stay stable until the ***finish*** signal is set high by the process.

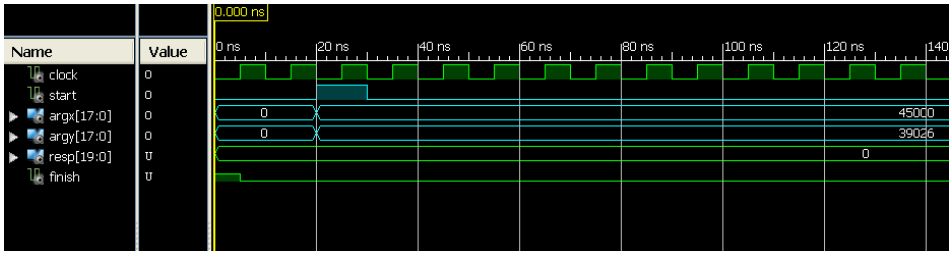

*Figure 3: timings of **start** and input signals*

The ***finish*** signal is set high for 1 clock cycle when the process terminates and ***resP[19:0]*** is valid. The ***resP[19:0]*** signal is valid until the next ***start*** signal is set high by the user or a ***reset*** is received by the process.

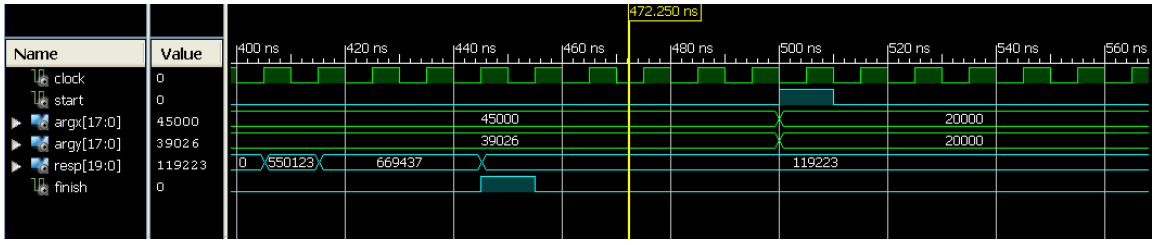

*Figure 4: timings of **finish** and **resP[19:0]** validity*

The ***reset*** signal, caught anytime on the rising edge of the clock, resets the core and set ***resP[19:0]*** to 0.

[2] The clock period is only chosen with the purpose to draw the waveforms.

Reference Documents

1. Xilinx LogiCORE IP DSP48 Macro V2.1 [DS754 March 1, 2011]
2. Xilinx LogiCORE IP Block Memory Generator V6.1 [DS512 March 1, 2011]

Support

QDESYS provides technical support for this LogiCORE product when used as described in the product documentation.

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Ordering Information

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Revision History

Date	Version	Description
13/07/2011	1.0	Initial QDeSys release.
22/12/2011	1.2	Added parameters for FPGA family
12/05/2012	1.3	Added Kintex 7 and Zynq support

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